Low Power and High Speed SAR ADC-A Review

Nishitha Palan, Nidhi Sampath, Pooja Vilekha Burujula

Abstract— **In the present technical era, with all the technological advancements in wireless communication and Complementary Metal Oxide Semiconductor (CMOS) scaling. It challenges analog designers to improve the Analog to Digital Converter (ADC) architectures. Thus leads their design to demand for a reduction in the power consumption. Along with it, it also calls for higher resolution, speed and smaller area. Analog to digital convertors are mainly power hungry compared to any other blocks in any architecture. Among the different Analog to digital convertors, Successive Approximation Register (SAR) Analog to digital convertor (ADC) is proven to provide results with lower power consumption and lesser area with higher speed and medium accuracy compared to others. So, in this paper, we discuss about the various approaches used in designing Successive Approximation Register Analog to digital convertor to provide an optimized design with low power and high speed.**

***Index Terms*— Calibration, comparator, high speed, low power**

I. INTRODUCTION

The global need for analog to digital converters at the receiver end have always been necessary. As most of the signals in real world are analog in nature. But the digital data which can be accessed, stored and processed easily as well as rapidly is been one of the concern in the digital world. Analog to digital convertor is a main component for designing a high speed, power and area limited systems.

Successive approximation register (SAR) ADCs show an admirable power efficiency for medium-resolution applications due to their high digital nature. There are many ADC architecture present out of which, successive approximation register is the best because of its low power consumption, medium speed, moderate resolution and low supply voltage. SAR ADC is most demanding in low power and high speed applications such as in biomedical field, wireless communications and IoT based applications.

II. SAR ADC WORKING PRINCIPLE

SAR ADC consists mainly of four blocks as shown in Fig 1, sample and hold circuit, comparator, successive approximation logic and digital-to-analog converter. The operation of SAR ADC is best explained using a binary search algorithm. A reference voltage from Digital to Analog Converter (DAC) is fed to the comparator along with a sampled input signal through the sample and hold circuit. The SAR logic outputs a binary code to DAC adjusting the output of the DAC which depends on the comparator output fed to the SAR approaching the input voltage. The digital output is based on the approximated output received at the end of conversion.

The rest of the paper is organized as follows. Section III describes the related works from various other clusters. The Section IV concludes the paper with some techniques proven to be effective in various papers.

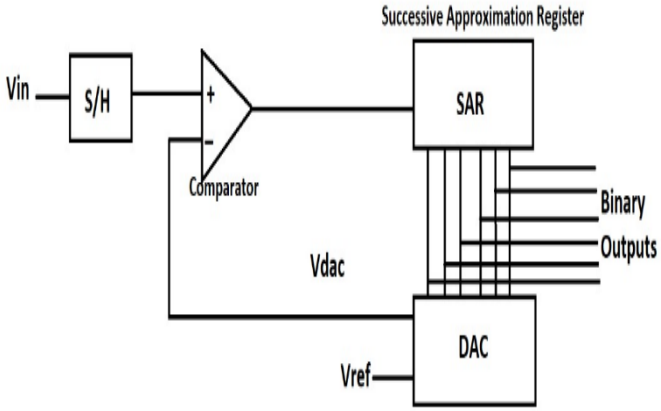

Fig 1. Block diagram of SAR ADC

III. LITERATURE REVIEW

In this section, we are elucidating the variety of approaches used in different works to make the design more optimized in terms of power, speed, area and resolution.

Yan Zheng et al., proposed a 13-bit 100MS/s SAR ADC. In this paper, a three stage comparator based inverter is implemented to enhance the speed. Also to keep the comparator noise low as it affects the speed. In addition to it, an improved asynchronous logic circuit with feedback is implemented to reduce the leakage current of the transistor. The proposed architecture has simple configuration and high digital nature because of which it is energy efficient. This methodology is fabricated in SMIC 14nm CMOS FinFET consuming 2.34mW power. The limitation in this paper is that the trade-off between noise and power in comparator is not linear. [1]

Sanjeev et al., proposed a single channel band pass SAR ADC architecture which can be ported into advance technologies to improve speed and to reduce power, because of its high digital nature. The proposed architecture in this work diminishes the drawbacks and also there are 5x improvements in energy efficiency that is associated with existing Band pass SAR ADC architecture. The off-chip

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implementation of Maximum Likelihood Estimation will allow us to check different noise transfer function. It also improves the signal-to-noise ratio. The prototype of the proposed ADC is fabricated in 65nm CMOS technology consuming 17uW power and BP-FoM of 29fJ/step for 100 KHz. The temperature limit has to be 60°C to avoid damaging of plastic components on the test-board. [3]

The work proposed by Guanhua Wang et al., presents a 1-GS/s 3.2-mW 8-bit SAR ADC implemented in 28-nm CMOS technology uses background-calibrated coarse and fine comparators to reduce the power consumption. The proposed SAR ADC architecture is shown below in Fig 2. The comparator approach here has a redundant DAC to control both the DAC settling errors and comparator errors. In this design, the 9th bit is not chosen to perform the offset calibration because the decision of the 9th bit is very close to the DAC reset cycle and would affect the calibration accuracy and instead the 7th bit and 8th bit is used. The total offset calibration area is 25% approximately of the total ADC area with a total offset calibration power consumption of 0.34 mW. By using the proposed reference comparator calibration scheme, the calibration time is removed from the SAR timing budget completely. The prototype ADC achieves the SNDR of 43.6 dB near Nyquist frequency with FOM 25.87 fJ/conversion-step.
[5]

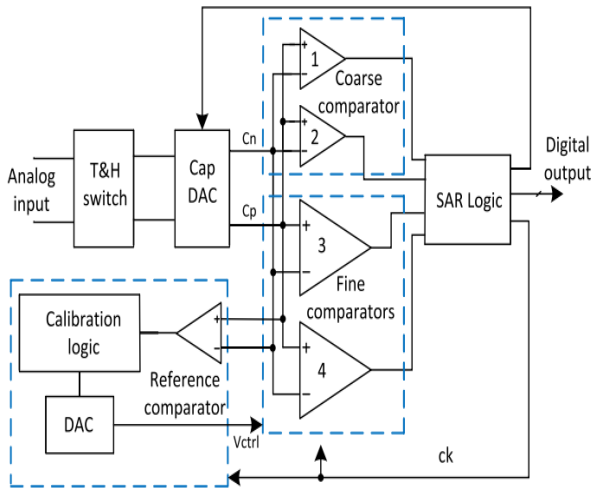

Fig 2. The architecture of SAR ADC presented by Guanhua Wang et al [5]

Naveen I.G and Savita Sonoli presented a 12 bit SAR ADC used for long battery life applications. A split based capacitor is used to increase the overall speed of the architecture. Furthermore in order to achieve high sampling linearity bootstrapped switches are used. The technique mentioned in this paper will overcome the utilization of more area, high power and high current consumption that is caused in 180nm, 90nm and 65nm technologies. This method was implemented in 45nm CMOS technology. This architecture consumed 46.367µW power and 4206.6µm² active area. To implement this architecture, it requires number of stages which increases the complexity of ADC. [6]
Haoyu Zhuang et al., presented a low-power and scaling friendly 9-bit noise shaping SAR ADC which is best suited for sensor applications with low duty cycle. In this paper the authors have proposed the use of passive switches and capacitors to perform residue integration and to perform the path gain, which consumes less power and is scaling friendly compared to operational trans-conductance amplifiers. Besides the proposed architecture, two new circuit techniques are proposed. A tri-level voting scheme and a multi-phase clock generator is designed to reduce the comparator noise. This prototype is fabricated in 40-nm CMOS process achieving a peak SNDR of 78.4db over a bandwidth of 262KHz. [7]

The author Andrea Di Salvo proposed a 12-bit SAR ADC for radiation detectors used in nuclear and particle physics. The bit value for each branch of the two divided sub arrays of DAC is one-half of the single ended counter-part. Here the implemented calibration technique belongs to the digital calibration class which is based on a perturbation injection and it uses the superposition principle of linear systems. This work was successfully synthesized in 65 nm and 110 nm CMOS technology devours a power of 3.08 mW and 5.66 mW utilising the cell area of 30µm² and 84µm². This work illustrated a spurious-free dynamic range of 75dB with 10.38 as effective number of bits. [8]

The author Jun-Eun-Park et al., proposed a voltage digital-to-analog converter (VDAC) and a rail to rail hybrid comparator to implement SAR ADC which is used for IoT applications. The proposed SAR scheme uses an oversampling technique and redundant error correction in place of sample and hold circuit. The Fig 3 below shows the block diagram of the proposed SAR ADC. Since the ADC exhibits non-linear transfer characteristics, to compensate the ADC nonlinearity effect this paper has proposed a soft calibration process. The ADC is fabricated in 28 nm CMOS process occupying the area of 0.002mm2. [9]

Jian Luo et al., 2019 proposed a 10-bit 2MS/s non-binary 2 bits per cycle time and voltage-based SAR ADC. It also consisted of low voltage and low power consumption. It was implemented in 130nm CMOS technology. This work utilizes the comparator timing information to obtain two bits information from the result of each comparison cycle. In the 2b/cycle architecture, a time comparator is used instead of a voltage comparator because they have simpler circuit designs with low power consumption. This improved architecture makes full use of the comparator delay information under low voltage conditions. The 2b/cycle quantization is an effective measure to improve the working speed and also can achieve a good FoM with the value 25.87 fJ/conversion-step. In the SAR cell, the quasi-dynamic latches are used to improve the speed and also reduces the delay. Although, due to the low power design, self-heating contributes a little on the delay. The above proposed ADC is suitable for energy limited applications such as sensing systems and implantable bio-medical devices. [10]

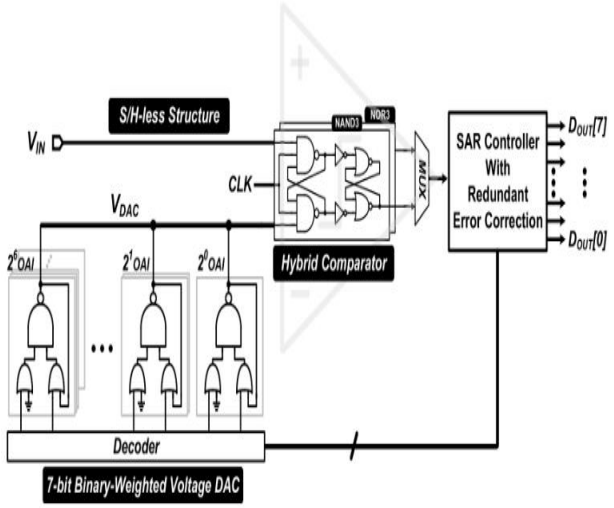

Fig 3. Block diagram of the proposed SAR ADC [10]

Mojtaba Bagheri et al., proposed a SAR ADC with stochastic mismatch calibration which is fabricated in 28nm CMOS technology that occupies the core area of 0.011mm². The prosed architecture of ADC with mismatched calibration is shown in the Fig 4. In this paper, the mismatch calibration circuit implemented is used to scale down the DAC to lower KT/C noise ratio, thus increasing the overall power efficiency of ADC. The stochastic quantization method is employed only when the residue voltage is lower than 1 LSB. In this research work, the prototype 10-bit SAR ADC, demonstrates calibration improvement in SNDR and SFDR of 11.5dB and 14.6dB. [11]

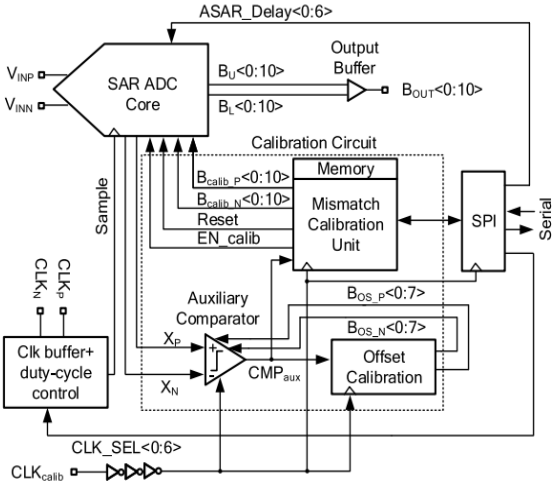

Fig 4 Overall architecture of ADC with mismatch calibration [11]

Aleksandr Gusev et al., presented a monotonic switching SAR ADC architecture which is designed and simulated in UMC065 design kit. The use of multi-step scheme is a tradeoff between area and efficiency without affecting the ADC and also provides 50% energy saving. In addition to it a proposed 4-step switched capacitor DC/DC converters allow to generate 2n equidistant voltage step to improve energy saving. The proposed method will save 43.35% area, assumed that the capacitor area is three times more. [12]

A maximum likelihood estimation-based SAR ADC was proposed to reduce the ADC noise and improve the overall energy efficiency by Akshay Jayaraj et al. In this work the accuracy estimated does not degrade with any other change in the values and thus proves to be a huge advantage compared to the previous existing ones. A 10-bit capacitive DAC and bottom-plate sampling is used in this ADC along with a comparator which consumes low power due to its small size. Therefore, a gain error correction was not required in this ADC. After the quantization for maximum likelihood estimation, the comparator was fired 18 times consuming 5µW power alone along with SAR logic out of 9µW and the remaining 4µW was consumed by DAC. The above power consumption was recorded after testing a chip with 1V supply using the sampling frequency of 1.28MHz with an SNDR of 62.5 dB and FOM of 4.9fJ/step. [13]

The authors Athanasios T. Ramkaj et al., presented a 1.25-GS/s 7-b single channel calibration free SAR ADC to obtain lowest FoM combined with lowest SNDR. In this research work, a triple-tail dynamic comparator is implemented to achieve both high speed and low noise. The schematic diagram of the proposed triple-tail comparator is shown in Fig 5. In order to minimize the performance degradation in the CDAC, three references are used in the CDAC which are decoupled on-chip. This paper introduces a technique called unit-switch-cap which simultaneously minimizes the Cw and Rw parasitic contribution in the CADC. This methodology is fabricated in 28-nm CMOS technology achieving a FoM value 34.4 fJ/conversion-step. [14]

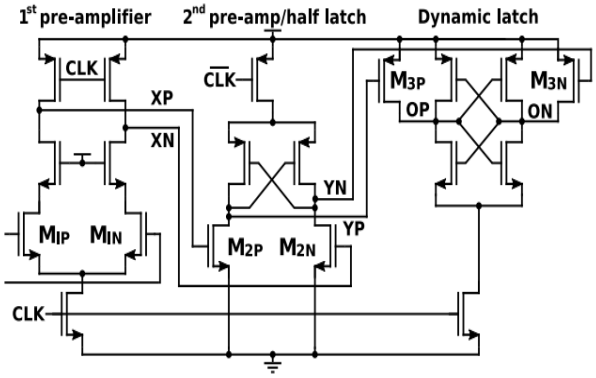

Fig 5 Schematics of triple-tail comparator [14]

Vijay Pratap Singh et al., proposed a 8-bit high speed and power efficient SAR ADC using a simple sample and hold circuit which has MOS as a switch to drive the clock signal and also a holding capacitor. The DAC used here has R-2R ladder structure because it is merely op-amp free which in turn helps in reducing the offset problem and kickback noise. In the SAR logic, a ring counter is used along with a SR flip-flop to get the nth bit. Here a double tail dynamic latch and proposed latch are used to devour less power of about 14.77µW and 3.93µW respectively. It also helps to attain high speed. This ADC design was implemented in 90nm CMOS technology with a supply voltage of 1.2V and with the clock frequency of 250MHz dissipating 0.98nW in total with

250MS/s sampling frequency. [15]

Shakeel Ahmad proposed an 8-bit SAR ADC which is implemented in 180nm technology. In this paper, a differential amplifier is used at the output of the S/H circuit in order to avoid the loading effect and also to reduce the noise effect in the comparator a differential amplifier is used. In addition to it, an R-2R ladder network is used to implement the DAC block in order to improve the precision. The comparator block consumes more power compared to the other block and the power dissipated is calculated to be 0.19mW. The power consumed by S/H circuit is almost zero and the overall power consumption of ADC is 0.75mW. [17]

Wang Jun and Zuo Yan introduced a low power 12-bit SAR ADC mainly for portable electroencephalography sensor. Here a technique called self-calibration is used in DAC with split capacitor charge distribution. Since, only capacitors are used for it, the power consumption is lower than others. Not only it reduces power but also improves the overall conversion accuracy, reduces the effect of capacitance error, eliminates the parasitic electric capacity and non-linear error due to capacitor mismatch. This methodology was implemented in 0.13µm CMOS obtaining SNDR of 71.47db by consuming 26µW of total power with supply voltage of 1.2V meeting the requirements of portable sensors. [18]

IV. Conclusion

This survey paper has explained different schemes used in different papers to design an optimized low power and high-speed SAR ADC. Along with power and speed, area and resolution were also considered and improvised based on the requirement for different applications. Among the four blocks in the SAR ADC, comparator is considered to be the most power-hungry block. So, to ensure that the design devours lesser power consumption along with the increase in speed, this paper suggests few schemes. Firstly, a novel energy efficient switching scheme is suggested for reducing the switching power devoured by the capacitor array [16]. In Fig 6, a VCM scheme (VCM refers to common-mode voltage which is half the value of VREF) is shown which is also used in the suggested switching scheme. All the top plates of the capacitors are connected to the input while the bottom plates are charger to 0, VREF, …., VREF during the sampling phase. By implementing this scheme, MSB is determined without the need of any energy consumption and thus by saving the overall consumption.

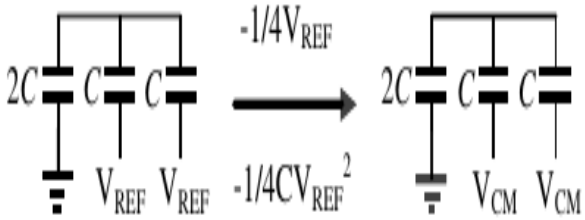

Fig 6 Demonstration of reducing negative switching energy [16]

Another scheme suggested by this review is on the comparator design. During the low supply voltage, the delay in the comparator decision increases, but when the delay is utilized as an advantage by quantizing 2bits/cycle, speed of the SAR ADC can be increased. Also, by using the comparator delay during the low supply voltage when combined with respective low voltage circuit design techniques, a good FOM value also can be obtained.

With respect to the design of the comparator, using a time-based comparator proves to be of an advantage because of the simple design, which also helps reducing power consumption and jitter contribution. The suggested time-based comparator is shown in Fig 8, as it can be understood that it is an SR latch and two completely symmetrical NAND2. Fig 9 shows the design of a voltage-based comparator, it consists of a pre-amplifier along with a dynamic latch comparator. Specially during low supply voltage, the dynamic comparator has few limitations with the resolution though it is known for its non-dynamic power consumption. A pre-amplifier serves from several to around 10-times magnification without consuming any static power. For the DAC, R-2R is preferred because of the simple design and only two resistances used throughout compared to the novel design. When a combination of two voltage-based comparator with one time-based comparator is designed in the SAR ADC along with the presence of the suggested energy efficient switching scheme and R-2R DAC, a desired result can be achieved.

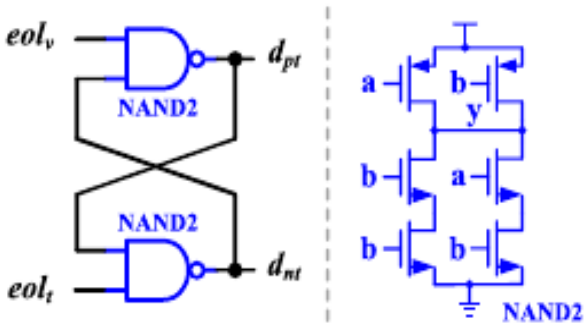

Fig 8 Schematic of time-based comparator. [10]

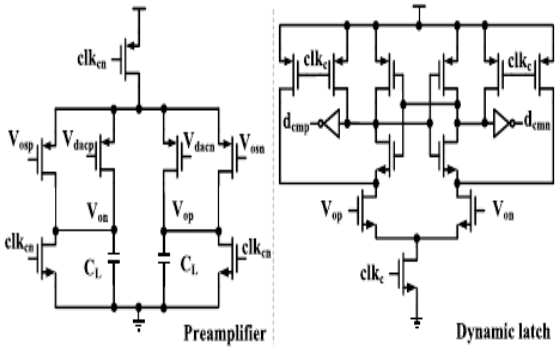

Fig 9 Schematic of voltage-based comparator. [9]

TABLE I

COMPARISON BETWEEN VARIOUS SAR ADCS BASED ON DIFFERENT PARAMETERS

Reference No.	A Switched Capacitor-Based SAR ADC Employing a Passive Reference Charge Sharing and Charge Accumulation Technique [2]	8fJ/Step Bandpass ADC With Digitally assisted NFT reconfiguration [3]	Design and Implementation of Energy Efficient SAR Analog to Digital Converter [4]	A Low Voltage and Low Power 10-bit non-binary 2b/Cycle Time and Voltage Based SAR ADC [10]	Maximum Likelihood Estimation Based SAR ADC [13]	An Energy Efficient Switching Scheme For Low Power SAR ADC Design [16]	Design of a low power 12bit SAR ADC with self-calibration [18]
Technology (nm)	180	65	90	130nm	65	180	130
Sampling Rate(S/s)	2K	2.43M	30K	2M	1.28M	100K	-
Power Consumption (W)	0.28 µ	17 µ	0.26 µ	3.4 µ	7 µ	0.0437 µ	26 µ
Supply Voltage (V)	1.8	1	0.8	0.5	1	0.6	1.2
SNDR (dB)	62.8	68.9	42.3	56.7	62.5	59.3	71.47
Resolution	11	-	8	10	10	10	12

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