Design of schematic synchronously clocked JK flip-flop using CMOS technology

Duy Khanh Pham

Abstract — ***Nowadays, CMOS technology has played a vital role in implementing high density, high-speed, and low-power VLSI systems. Designing IC chip basically consists of a numerous numbers of logic gates which are integrated inside. Reducing the power dissipation of the circuit is always a big challenge to any circuit designer. There are many different techniques to reduce power consumption based on circuit level, architecture, layout design, and process technology. Universal JK flip-flop (JK-FF), also known as a latch circuit, is an improved version of the SR flip-flop and can be operated with both high active inputs. JK-FFs is widely used in electronic circuits with the main aim to store the state information of the device. The major applications of JK-FF are used for shift registers, data storage (RAM), data transfer, counters, frequency dividers, storage registers, event detectors, data synchronizers, PWM and computer applications. The current paper aims to design schematic synchronously clocked JK-FF using CMOS technology with the number of transistors used less than some other design methods. The schematic, simulation and layout of the proposed design are performed on Cadence software.***

Index Terms *— Flip-flop, CMOS technology, VLSI design, low power, Cadence.*

I. INTRODUCTION

For designing IC chip the circuit consist of many numbers of logic gates which are integrated inside. The minimization of power dissipation in any circuit has always been a big challenge for any circuit designer. There are many related works which are already carried out by different groups with different techniques like bipolar junction transistor, CMOS technology, BiCMOS technology etc. Designers are able to work on more transistors onto the same die because of the shorter size of the CMOS as per Moore's law.

Latches and Flip-flops are the sequential circuits that stores 1 and 0 state called logic states. Latches works on level triggered while flip-flops works on edge triggred. A flip-flop is a bistable circuit which give the output in response to a reference pulse. The data stored in flip-flops on the rising and falling edge of the clock signal is applied as the inputs to other sequential circuits. Those flip-flops which stores data on both the rising and falling of the clock signal are termed as double edge triggered flip-flops and those flip-flops that stores data either on the rising or falling edge are known single edge triggered flip-flops.

JK-FF is a flip-flop, also known as a latch circuit, that can be either active-high or active-low based on the signal applied. It is an improved version of the SR flip-flop and prevents the circuit from going in an invalid state. As the name suggests, it helps the circuit toggle between two states. The JK flip-flop is named after his inventor known as *Jack Kilby* from Texas Instruments. The JK flip-flop is also widely known as a programmable flip-flop as it can disguise other flip-flops based on the inputs applied. JK-FF is a universal flip-flop that makes the circuit toggle between two states and is widely used in shift registers, counters, PWM and computer applications. JK-FF is widely used in electronic circuits with the main aim to store the state information of the device. Following are the major applications it can be used for Shift Registers, Data storage (RAM), Data transfer, Counters, Frequency Dividers, Storage Registers, Event detectors, Data Synchronizers, Bounce elimination switch, etc.

II. DESIGNING CMOS CIRCUIT OF JK FLIP-FLOP

JK-FF can be considered as an improved version of SR flip-flop. The JK-FF can operate when both inputs are at high level while the SR-FF is impossible. Understanding the suitability of flip-flop and choosing the right flip-flop topology are important in designing VLSI circuits using CMOS technology. That is to meet the demands of designs with high speed, low power, and high performance [1],[2],[15],[16], [16].

The JK-FF in this design has 3 data inputs: J, K, clock input (Clk) and 2 outputs: Q and $\overline{Q}$ (Q bar) . The logic structure of the JK Flip-Flop used in the design is shown in Figure 1.

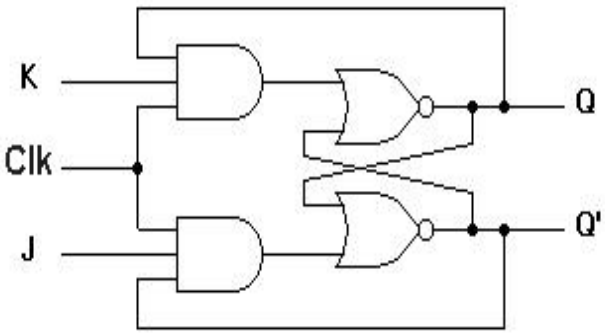

Fig. 1: The logic diagram of JK-FF based NOR gates

The operating principle of JK-FF is shown in Table 1. with Q_n and Q_{n+1} are the current and the next output state of the flip-flop, respectively.

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Table 1. The truth table of JK flip-flop

J	K	Clk	Q_n	$\overline{Q_n}$	Q_{n+1}	$\overline{Q_{n+1}}$	Description
0	0	↑	0	1	0	1	Hold
			1	0	1	0	
0	1	↑	0	1	0	1	Reset
			1	0	0	1	
1	0	↑	0	1	1	0	Set
			1	0	1	0	
1	1	↑	0	1	1	0	Toggle
			1	0	0	1	

2.1 The basic structure of the CMOS circuit at gate level

The basic structure of the CMOS circuit consists of two parts - the PDN circuit and the PUN circuit, linked together as shown in Figure 2.[3],[5]. In general, a static CMOS gate has an NMOS pull-down network to connect the output to 0 (GND) and PMOS pull-up network to connect the output to 1 (V_{DD}). The networks are arranged such that one is ON and the other OFF for any input pattern.

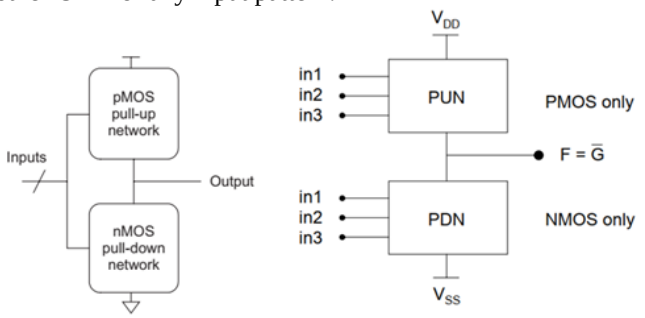


Fig. 2: The basic structure of a CMOS circuit

In digital logic circuits, NMOS and PMOS act as switches. When the gate of an NMOS transistor is 1 (high level), the NMOS will be ON, and there is a conducting path from drain to source. When the gate is low, the NMOS transistor is OFF and almost zero current flows from drain to source. With PMOS it will be the opposite, being ON when the gate is low and OFF when the gate is high. When connected in series or parallel the NMOS or PMOS together, they will perform basic operations in logical algebra such as AND and OR [5].

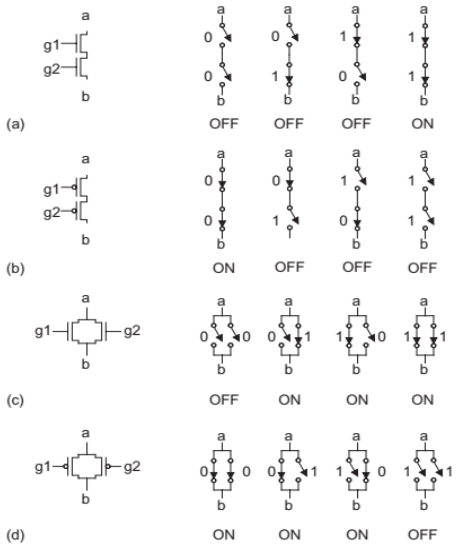


Fig. 3: The circuit performs AND and OR operations when connecting NMOS or PMOS in series and parallel

Two or more transistors in series are ON only if all of the series transistors are ON. Two or more transistors in parallel are ON if any of the parallel transistors are ON. By using combinations of these constructions, CMOS combinational gates can be constructed.

2.2 Designing the CMOS circuit for Q output of JK-FF

From the logic diagram of the JK-FF circuit in Figure 1, we can write the logic equation for the two outputs of flip-flop:

- Q output: $F_1 = Q = \overline{Clk.K.Q + \overline{Q}}$ (1)

- Q bar output: $F_2 = \overline{Q} = \overline{Clk.J.\overline{Q} + Q}$ (2)

2.2.1 Designing the PUN circuit

Convert the logic equations (1) to form: $F_1 = f(\overline{Clk}, \overline{K}, \overline{Q})$

$$F_1 = Q = \overline{Clk.K.Q + \overline{Q}} = (\overline{Clk} + \overline{K} + \overline{Q}).\overline{\overline{Q}} \quad (3)$$

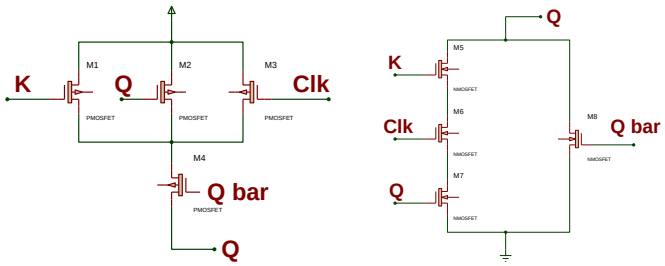
The PUN circuit for Q output of JK-FF consists of 3 PMOS transistors connected in parallel with the corresponding inputs are *Clk*, *K*, *Q* and in series with 1 PMOS transistor with input is $\overline{Q}$.

2.2.2 Designing the PDN circuit

Convert the logic equations (1) to form: $\overline{F_1} = f(Clk, K, Q)$

$$\overline{F}_1 = \overline{Q} = \overline{\overline{Clk.K.Q + \overline{Q}}} = Clk.K.Q + \overline{Q} \quad (4)$$

The PDN circuit for output Q of JK-FF consists of 3 NMOS connected in series with inputs are *Clk*, *K*, *Q*, and parallel to 1 NMOS with input is $\overline{Q}$.



a) b)

Fig. 4: The structure of the PUN circuit (Figure 4a) and the PDN circuit (Figure 4b) for Q output of JK-FF.

Combining the two structures above we have a CMOS circuit for the Q output of JK Flip-flop as shown in Figure 5.

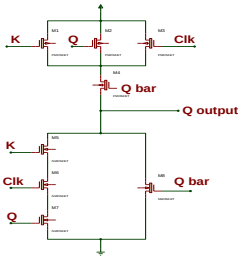


Fig. 5: The CMOS circuit for the Q output of JK flip-flop

2.3 Designing the CMOS circuit for Q bar output of JK-FF

Similarly, to design the CMOS circuit for the Q bar output of JK flip-flop, we also design the PUN and PDN circuits and then combine them together.

The logic function for Q bar output:

$$F_2 = \overline{Q} = \overline{Clk.J.\overline{Q} + Q}$$

2.3.1 Designing the PUN circuit

Convert the logic equations (2) to form: $F_2 = f(\overline{Clk}, \overline{K}, \overline{Q})$

From the equation for the output $\overline{Q}$ above, we convert to

$$F_2 = \overline{Q} = \overline{Clk.J.\overline{Q} + Q} = (\overline{\overline{Clk}} + \overline{J} + \overline{\overline{Q}}).\overline{Q} \quad (5)$$

The PUN circuit for $\overline{Q}$ output of JK-FF consists of 3 PMOS transistors connected in parallel with the corresponding inputs *Clk, J,* $\overline{Q}$ and series with 1 PMOS with input is Q.

2.3.2 Designing the PDN circuit

Convert the logic equations (2) to form: $\overline{F_2} = f(Clk, K, Q)$

$$\overline{F}_2 = \overline{\overline{Q}} = \overline{\overline{Clk.J.\overline{Q} + Q}} = Clk.J.\overline{Q} + Q \quad (6)$$

The PUN circuit for $\overline{Q}$ output of JK-FF consists of 3 PMOS transistors connected in series with the corresponding inputs *Clk, J,* $\overline{Q}$ and parallel with 1 PMOS with input is Q.

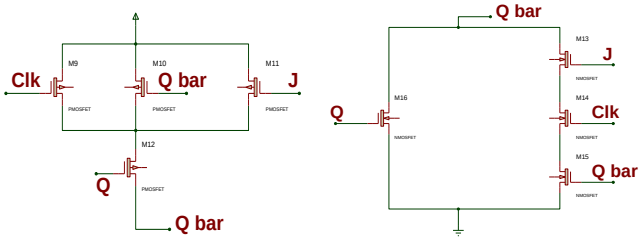


Fig. 6: The structure of the PUN circuit (Figure 6a) and the PDN circuit (Figure 6b) for Q bar output of JK-FF.

Combining the two structures above we have a CMOS circuit for the Q bar output of JK Flip-flop as shown in Figure 7.

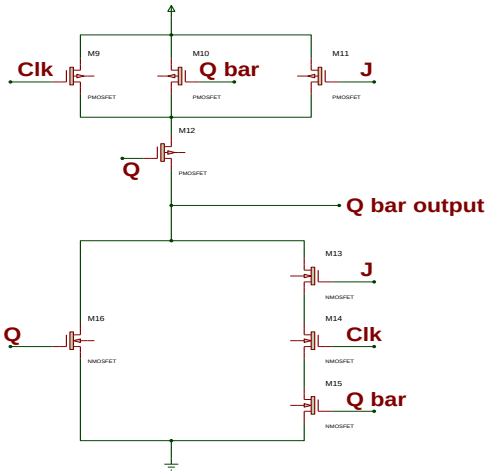


Fig. 7: The CMOS circuit for the Q bar output of JK-FF.

Combining above 2 circuits were designed for Q and Q bar output, we have the schematic synchronously clocked JK flip-flop using CMOS technology.

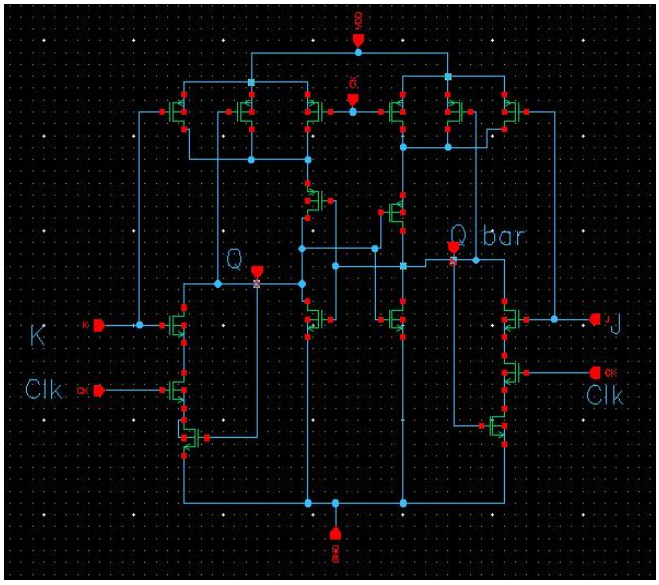


Fig. 8: The schematic synchronously clocked JK flip-flop using 90nm CMOS technology.

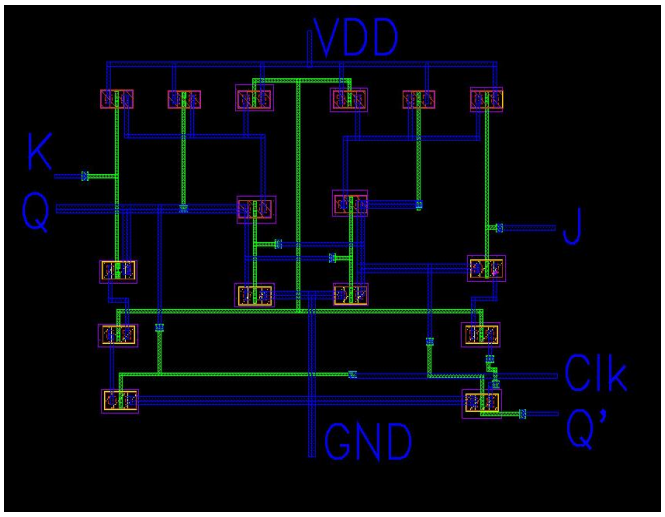


Fig. 9: The layout of JK flip-flop using CMOS technology.

III. RESULTS AND DISCUSSION

Based on the principle of CMOS circuit design, from designing individual parts of PUN and PDN circuits and combining them together, the author has come up with the design of JK Flip-flop using CMOS technology, one of the technology that is widely used in IC fabrication nowadays. In many previous related studies, the authors have hardly shown how to design the CMOS circuit diagram of a known logic function. Compared with some other design methods such as TG (Transmission Gates), CPL (Complementary Pass Transistor Logic) or standard CMOS, the design given in this paper has less number of transistors used, therefore the power consumption of the circuit will be smaller, the chip surface area will be smaller and the delay time of the circuit will be reduced [13].

Table 2. Compare the number of transistors used to design JK-FF using several different methods.

Method	The standard CMOS JK-FF circuit	The CMOS JK-FF circuit using TG	The CMOS JK-FF circuit using CPL	The CMOS JK-FF cirrcuit in the article
The number of transistors used	32	40	54	16

The simulation results also show the correctness of the circuit design.

Fig. 10: The simulation results of the pulse signals at inputs and outputs of JK flip-flop.

IV. CONCLUSION

The research has shown a method to design the JK Flip-flop using CMOS technology and the results show that the number of transistors used in the design is less than some other methods. This result helps students of engineering and technology universities, especially in the field of CMOS VLSI IC design, have a method of designing CMOS circuits from combinational logic circuits to sequential logic circuits. Therefore, they can be to design logic circuits with more complex structures using in practical applications. However, in this research, the author has not given a table specific parameters about the average power consumption, maximum power dissipation, the system delay, surface area of chip integration. These issues will need to interested in the next research.

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