

Review on Low Power energy efficient VLSI circuits using Adiabatic logic

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Abstract— The ever-growing number of transistors integrated on a chip and the increasing transistor switching speed in recent decades has enabled great performance improvement in computer systems by several orders of magnitude. Unfortunately, such phenomenal performance improvements have been accompanied by an increase in power and energy dissipation of the systems. Higher power and energy dissipation in high performance systems require more expensive packaging and cooling technologies, this in turn increase cost, and decrease system reliability. Demands for low power electronics have motivated researchers to explore new approaches to reduce power consumption and energy dissipation in VLSI circuits. The classical approaches of reducing power consumption, energy dissipation in conventional CMOS circuits included reducing the supply voltages, node capacitances, switching frequencies and recycling energy back to power supply respectively. In this paper a review about subthreshold operation, adiabatic logic and adiabatic logic in subthreshold region.

Index Terms— Adiabatic, CMOS, Energy Recovery, Power Consumption, Subthreshold, VLSI

I. INTRODUCTION

Recently, power consumption has been a fundamental constraint in both high-performance and portable, energy-limited systems. In conventional CMOS circuits, power dissipation primarily occurs during device switching. A sudden flow of current through channel resistive elements results in half of the supplied energy being dissipated at each transition. In CMOS technology, as $E_{diss} = \frac{1}{2}C_L V_{DD}^2$, research is focused on how to reduce V_{DD} and C_L to reduce energy dissipation. However, power dissipation can also be reduced by reducing the current flow in to the transistors.

In subthreshold logic, device sizing is done in such a way that they are operated with $V_{DD} < V_{th}$. In this weak inversion region, the leakage current or the subthreshold current is considered the computation current. The exponential I-V relationship in the subthreshold region of operation increases the current gain. However, it is to be pointed out that, although the switching power is greatly reduced, subthreshold circuit operations are intended mainly for medium throughput applications. Additionally, due to the exponentially increasing current gain, the sensitivity of the circuit to the process and temperature variations increases.

Nevertheless, the robustness of the circuit has been improved by different circuit level and device level techniques.

On the other hand, in the adiabatic logic, a time varying supply clock, called as power-clock is used, that reduces the voltage drop across the device at any time. The majority of the energy spent on charging the nodal capacitance is recycled back to the supply clock every time and is not dissipated to the ground as it occurs in CMOS. Hence, these circuits are called as Adiabatic circuits. This energy recovery property greatly reduces the switching power of the digital circuits.

Low-power circuit systems achieved by implementing the concept of adiabatic switching [1] and energy recovery have been widely applied, and various energy-recovery circuits with adiabatic circuitry for ultra-low power implementation have been presented. The essential idea of adiabatic charging is to design a circuit that allows all the nodes to be charged or discharge data constant current. Power dissipation is minimized by decreasing the peak current flow through transistors. This flow is accomplished by using ramp-like power/clock signals. The system draws some of the energy that is stored in the capacitors during a given computation step and uses this energy in subsequent computations.

II. SUBTHRESHOLD OPERATION

In digital circuits, power is needed to charge the load capacitance C_L of each logic node at the switching frequency f . This dynamic power consumption can be expressed as

$$P_{dyn} = V_{DD} \cdot f \cdot C_L \cdot \Delta V_{DD} \quad (1)$$

where V_{DD} is the supply voltage and ΔV_{DD} is the logic voltage swing, smaller or equal to V_{DD} . Thus the dynamic power can be reduced by reducing ΔV_{DD} , but this gate voltage swing is needed to ensure a sufficient current ratio I_{On}/I_{Off} in the transistors producing the transitions. Indeed, the on-current I_{On} must be large enough to ensure transitions at the required speed, and I_{Off} should be as small as possible to limit the static power consumption $P_{stat} = I_{Off} \cdot V_{DD}$ between transitions. The swing needed to achieve a given value of I_{On}/I_{Off} can be reduced by reducing the gate voltage overhead, until it becomes minimum when weak inversion is reached. Logic circuits based on transistors operated in weak inversion (also called subthreshold) therefore offer minimum possible operating voltage thereby minimum P_{dyn} for a given P_{stat} .

The drain-to-source current I_{DS} of n-channel MOS transistors operated in weak inversion can be expressed as

$$I_{DS} = I_S \exp \left[\frac{V_{GS} - V_T}{nU_T} \left(1 - \exp \left[\frac{-V_{DS}}{U_T} \right] \right) \right] \quad (2)$$

where $n > 1$ is the subthreshold swing coefficient or slope factor of the transistor (practically always below 1.6), V_{GS} and V_{DS} the gate to source and drain to source voltages, V_T is the gate to source threshold voltage and I_S is the specific current given by

$$I_S = 2n\mu C_{ox} U_T^2 (W/L) \quad (3)$$

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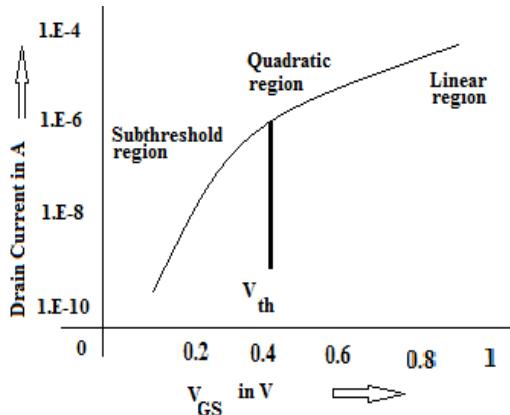


Fig.1.Exponential behavior of drain current in weak inversion region or subthreshold region

where μ is the carrier mobility, C_{ox} the gate oxide capacitance per unit area, $U_T = kT/q$ and W/L is the width-to-length ratio of the channel.

An added consequence of the subthreshold region is the decrease in the input gate capacitance, C_i given by

$$C_i = \text{series}(C_{ox}, C_d) \parallel |C_{if}| \parallel |C_{of}| \parallel C_{do} \quad (4)$$

Here, C_{ox} , C_d are the oxide and depletion capacitances, C_{if} and C_{of} are the fringe capacitances and C_{do} is the overlap capacitance. The second order effects of the MOS devices are also less pronounced in the subthreshold region. The subthreshold currents are weaker and hence, the time taken for charging and discharging the nodal capacitance is longer, as given by

$$T_d = C_L V_{DD} / I_{On} \quad (5)$$

Thus, operating the devices in the weak inversion region exhibits several benefits such as:

1. High current gain
2. Low power dissipation
3. High noise margin
4. Low input gate capacitance
5. Reduced gate tunneling current, Gate induce drain leakage and reverse biased diode leakage

However, the sensitivity of the subthreshold circuits to the PVT variations and the low throughput of the devices operating in the subthreshold regime are major obstacles that need to be eradicated to acquire the benefits.

III. ADIABATIC SWITCHING

Consider a conventional CMOS inverter circuits and its equivalent model using resistive-switch network as shown below.

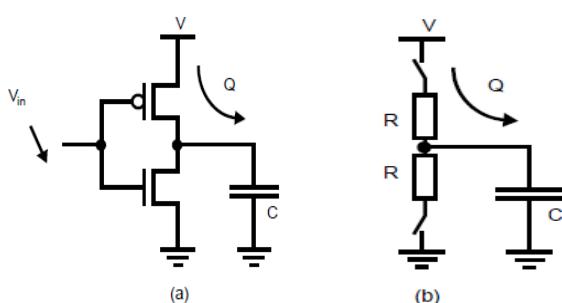


Fig.2 a)C of CMOS inverter charged to Power supply b) Idealized resistive switch representation of CMOS inverter

When the input, V_{in} is low, the pMOS device turns on, and the linear load capacitance C is charged from 0 to V . The total amount of energy delivered by the power supply is $Q.V$. The energy stored on the capacitor is $\frac{1}{2}C.V^2$. The difference between the delivered energy and the stored energy is dissipated in the PMOS switch. Now, if the input switches from 0 to 1, in steady-state condition the NMOS channel is on, the PMOS off. Charge stored on the output capacitance is then dissipated via the NMOS device to ground. The energy dissipation of a switching event in a static CMOS gate is given as

$$E_{CMOS} = \alpha \cdot \frac{1}{2}C.V^2 \quad (6)$$

where α is the switching probability, as there is no dissipation, except leakage losses in static CMOS gates, if there is no switching event at all. Different approaches are useful to reduce the energy dissipation in static CMOS. Reducing the capacitive load, C is strongly limited by the technology and its intrinsic device capacitance. But wiring capacitance can be reduced by choosing a proper architecture and a carefully designed layout. Reducing the voltage supply V is a very powerful method to reduce the power dissipation, but as downside the performance is degraded.

In contrast to conventional CMOS Adiabatic Logic does not abruptly switch from 0 to V (and vice versa), but a voltage ramp is used to charge and recover the energy from the output. In adiabatic charging, capacitor is charge by the time varying power supply. For convenient we take ramp type voltage source $V(t) = V/T$, where V is the peak voltage of power supply and T is the time period. At any instant of time the current, $i(t)$ is given by

$$i(t) = \frac{VC}{2T} (1 - e^{-(t/RC)}) \quad (7)$$

Energy dissipated across the resistor during charging is given as

$$E_{diss} = \int_0^T i^2(t) R \, dt = \frac{(RC)}{T} C.V^2 \quad (8)$$

Upon comparing Energy dissipation of conventional CMOS (let $\alpha=1$), E_{CMOS} as given in equation 6 with Energy dissipation of CMOS using adiabatic charging principle, E_{diss} as given in equation 8 it is observed that E_{diss} can be lower than E_{CMOS} if T is long enough and in turn it may be made arbitrarily small by further extending the charging time.

IV. ADIABATIC LOGIC FAMILIES

This section presents the incremental construction of a logic style, which allows fully adiabatic operation. The construction of a buffer/inverter circuit using Energy Charge Recovery Logic(ECRL) and Positive Feedback Adiabatic Logic (PFAL) are shown in Figure 3 and Figure 7 respectively. Figure 4 shows the power clock signal which varies with time t . Figure 6 shows four phase power clock signal.

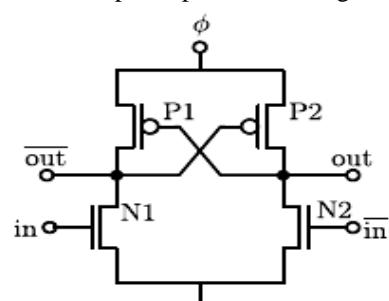


Fig.3 Energy Charge Recovery Logic(ECRL) buffer/inverter

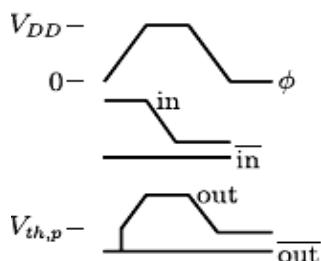


Fig.4.Power clock signal, input and output signals of ECRL buffer

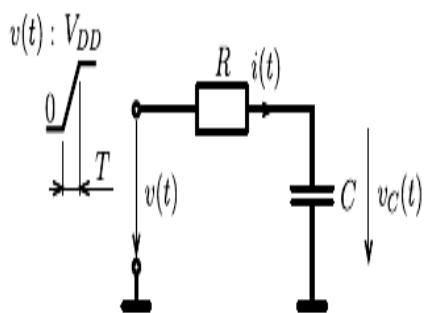


Fig.5 Equivalent circuit showing the Adiabatic charging of C through a ramp type power clock signal,

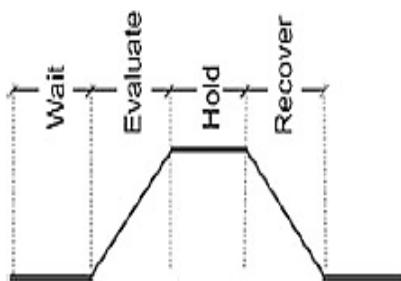


Fig.6.Four phase power clock

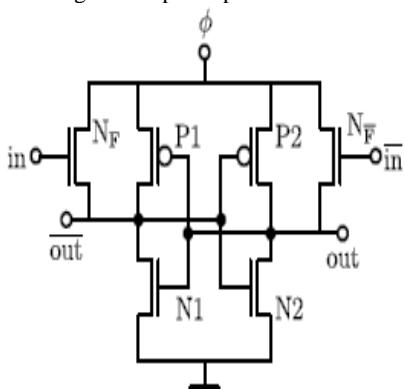


Fig.7.Positive Feedback Adiabatic Logic (PFAL) buffer/inverter

V. ADIABATIC LOGIC IN SUBTHRESHOLD

Region

Extending the subthreshold logic to adiabatic circuits can improve power efficiency of the energy recovery circuits for ultra-low power operation besides deriving several benefits from each of the low power schemes. In the adiabatic subthreshold mode of operation, i.e., the adiabatic structures are operated in the weak inversion region. The adiabatic structures are device sized for subthreshold operation and power clock PCLK voltage is held below the threshold value

VT for operation in the weak inversion region. This novel methodology acquires most of the merits of both the low power schemes which is listed as below.

1. The dynamic power dissipation $P_{dyn} = \alpha C_L V_{DD}^2 f$ is minimized as the nodal capacitance C_L is reduced by device sizing due to the reduction in the gate capacitances, V_{DD} being less than the threshold voltage and the power-clock period T being longer.
 2. Besides, absolute energy recovery made possible through the use of time varying power clock improves the power efficiency to a greater extent.
 3. Non-adiabatic power dissipation may also be brought down further.

VI. CONCLUSION

In this paper a review on low power mechanisms for VLSI circuits using subthreshold, adiabatic principles and subthreshold adiabatic logic is presented.

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