Emerging NanoFETs and Electrostatics Influencing Nanoscale Transistors: A Review

Deepthi Amuru, Dr.K.Ragini, Dr.P.ChandraSekhar Reddy

***Abstract*— As the dimensions of transistors shrink, the close proximity between the source and drain reduces the ability of the gate electrode to control the potential distribution and the flow of current in the channel region because of which undesirable short channel effects starts plugging in MOSFETs. For all practical reasons, it seems to be impossible to scale the dimensions of classical bulk MOSFETs below 20nm. To satisfy Moore's law in nanometer regime, the evolving nanotransistors are the promising alternatives to the planar MOSFETs. Nanotransistors reduce the short channel effects with improved device performance in terms of reduced power supply, power dissipation, leakage currents and improved scalability. This paper discusses about the challenges for scaling the transistors in nanoscale regime and also gives an insight on various types of emerging nanotransistors.**

***Index Terms*— Bulk MOSFETs, SOI, SCEs, MGFETs, FinFETs.**

I. INTRODUCTION

Short channel effects (SCEs) arise in MOSFETs with narrow channel lengths in which the drain potential influence the electrostatics of the channel and consequently gate loses control over the current flowing in the channel. Due to which gate is unable to shut off the current completely in the channel during OFF condition of the MOSFET. That causes leakage current (I_{off}) to flow in the device which in turn is responsible for the increased power dissipation [1], [2]. To improve the portability of an electronic device with longer battery life, there is a necessity to reduce the power dissipation as well as power consumption of that device. However, scaling the supply voltage is limited by scaling the threshold voltage of the transistors due to the exponentially increase in leakage current. For energy-efficient integrated circuit design new methods have to be explored to reduce I_{off} of the MOSFET.

The short channel effects are attributed to the limitation imposed on electron drift characteristics in the channel and the modification of threshold voltage due to shortening channel length. The SCEs can be distinguished as sub threshold leakage current (I_{off}), sub threshold slope, mobility degradation, threshold voltage roll-off, DIBL (Drain Induced Barrier Lowering), drain- punch through and hot carrier effects [3], [4]. Their influence can be reduced by reducing the depletion depth through an increase in doping concentration in the channel. SCEs can also be minimized by decreasing the junction depth and gate oxide thickness which help alleviate this problem by increasing gate capacitance C_g. In modern devices, however, practical limits on the scaling of the junction depth and gate oxide thickness lead to a significant increase in gate leakage current and Gate Induced Drain Leakage (GIDL) [5].

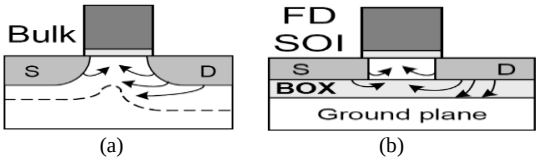
In a continuous effort to increase the current drive and better controlled SCEs, Multiple gate transistors FETs (MGFETs) have evolved. MGFETs are an alternative to planar MOSFETs demonstrating better screening of drain potential from the channel by employing additional gate(s) which provide higher gate-channel capacitance. This makes MGFETs superior to planar MOSFETs in short channel performance metrics.

The paper is organized as follows: In Section II electrostatic integrity in bulk and SOI MOSFETs is discussed. Followed by the details of EIF factor and its influence on reducing SCEs in case of bulk, FDSOI and DG MOSFETs in section III. In Section IV, classification of Multi gate FETs is discussed with the details of construction and features of various types of FETs. We review the different types of FinFETs and their classification depending on the asymmetries added to them in section V. A brief on digital circuit design using FinFETs and the tools required for simulation is dicussed in section VI. Followed by conclusion in section VII.

II. ELECTROSTATIC INTEGRITY

In a bulk device, the electric field lines propagate through the depletion regions associated with the junctions (fig 1a). The influence of electric field lines in the body can be reduced by decreasing the junction depth. When compared to bulk MOSFET, SCEs can be reduced in Fully-depleted Silicon-on-insulator (FDSOI) MOSFETs by using a thin buried oxide and an underlying ground plane. However, this approach has the influence of increased junction capacitance and body effect [6].

The device configuration of the double gate transistor structure shown in fig 1(c) more efficiently reduces the threshold voltage roll-off in short channel devices [7]. In the shown double-gate device, both the gates are tied together. The electric field lines from source to drain underneath the device terminate on the bottom gate electrode and cannot therefore reach the channel region. Only the field lines that propagate through the silicon film itself can encroach on the channel region and degrade short channel characteristics. This encroachment can be reduced by reducing the Si film thickness.



(a) (b)

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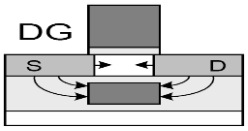


(c)

Fig 1: Influence of electric field lines from source to drain on the channel in different types of MOSFETs. (a) Bulk MOSFET (b) FDSOI with thin buried oxide and a ground plane (c) Double-gate MOSFET

The Multi gate transistors using Silicon-on-insulator technology show better device characteristics than planar technology [8]. FDSOI SOI devices have a better electrostatic coupling between gate and the channel. This results in a better linearity, sub threshold slope, body coefficient and current drive. MOS transistors have evolved from classical, planar, single-gate devices to three-dimensional devices with multi-gate structures.

Under multi-gate structures, double-gate, triple-gate or quadruple gate, MIGFET (Multiple Independent Gate FET), MuGFET (Multiple-Gate FET) technologies have evolved.

III. ELECTROSTATIC INTEGRITY FACTOR

Electrostatic Integrity factor (EIF) depends on device geometry and is a measure of the way the electric field lines from drain influence the channel region thereby causing SCE effects. The EIF can be obtained by applying Voltage Doping Transformation (VDT) model to bulk, FDSOI and double-gate MOSFETs (DGMOSFETs) [9].

$$EIF = \left[1 + \frac{x_j^2}{L_{el}^2}\right] \frac{t_{ox}}{L_{el}} \frac{t_{dep}}{L_{el}} \qquad (1)$$

Of a bulk device

Where, L_{el} is the effective channel length, t_{ox} is the gate oxide thickness, x_j is the source and drain junction depth, t_{dep} is the penetration depth of the depletion region underneath the gate in a bulk MOSFET.

The equivalent factor can be obtained for a FDSOI by noting the junction depth is equal to the silicon film thickness t_{si} and the gate field in the channel region penetrates into the depletion Si film and extends to some depth in the buried oxide, λ_{tbox}.

$$EIF = \left[1 + \frac{t_{si}^2}{L_{el}^2}\right] \frac{t_{ox}}{L_{el}} \frac{t_{si}+\lambda_{tbox}}{L_{el}} \qquad (2)$$

Of a FDSOI MOSFET

In a double-gate device, the effective junction depth and the effective gate field penetration for each gate is equal to $t_{si/2}$ which yields

$$EIF = \frac{1}{2}\left[1 + \frac{t_{si/4}^2}{L_{el}^2}\right] \frac{t_{ox}}{L_{el}} \frac{t_{si/2}}{L_{el}} \qquad (3)$$

Of a double gate MOSFET

EIF should be minimum to keep SCEs under control. This can be achieved by reducing the thickness of the device, either by reducing the junction depth x_j and depletion width t_{dep} in the bulk device; by reducing the Si film thickness t_{si} and buried oxide thickness t_{ox} in a FDSOI device; by reducing Si film thickness in DGMOSFET. By EI point of view, DGMOSFET has the natural advantage of looking twice as thin as equivalent FDSOI transistor. Because thin-film SOI devices deliver better EI than bulk MOSFETs, SOI devices can be used at shorter channel lengths while keeping acceptable DIBL values. The use of DG devices allows one to reduce gate length even further[10].

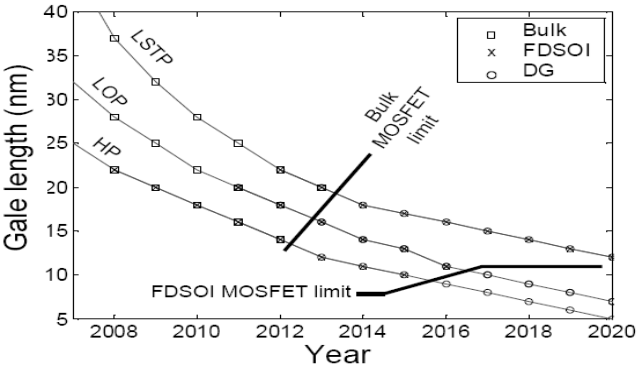


Fig 2: Evolution of gate length predicted by ITRS for high performance, Low operating power and low standby power digital circuits.

From the figure 2, the conclusion can be drawn that bulk transistors run out of stream once they reach a gate length of 15-20nm[11]. FDSOI can be until 10nm but smaller gate lengths can be only achieved by the DG structure.

IV. CLASSIFICATION OF MULTI-GATE MOSFETs

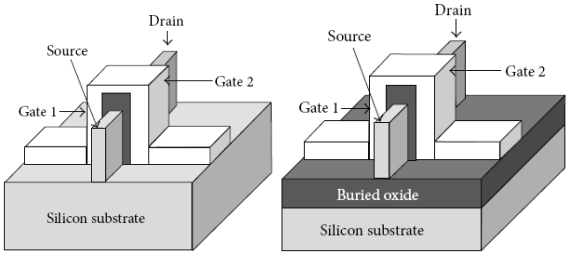
Multi-gate MOSFETS has more than one gate because of which the control of gate on channel increases and it helps to mitigate SCEs. A double-gate refers to single gate electrode that is present on two opposite sides of the device. Similarly triple-gate refers to single gate electrode that is folded over three sides of the transistor. MIGFET has two gate electrodes that can be biased with different potentials.

Table I: Different types of SOI Multi-gate transistors

Acronym	Type
MuGFET	Multiple/Multi gate FET
MIGFET	Multiple Independent Gate FET or four terminal (4T) FET
DGFET	Double Gate FET
3T FET	Triple gate FET
Quadruple-gate FET	Wrapped-around Gate FET Gate-All-Around(GAA) FET Surrounding Gate FET
FinFET	DELTA (fully Depleted Lean channel TrAnsistor)
FDSOI	Fully Depleted SOI
PDSOI	Partially Depleted SOI
DTMOS (Dual Threshold varied MOS)	VTMOS (Varied Threshold MOS) MTCMOS(Multiple Threshold CMOS) VCBM(Voltage-Controlled Bipolar MOS) Hybrid Bipolar-MOS Device

MGFETs can be fabricated on bulk wafer or on an SOI. The advantages of SOI technology come from its buried oxide (BOX) layer. With the reduction of the parasitic capacitances, SOI devices yield improved switching speed and reduced power consumption. The operating speed is also improved

since the isolated channel from substrate bias prevents the threshold voltage of stacked SOI transistors. They also offer tighter transistor packing density and simplified processing. The structural composition of bulk and SOI technologies is shown in fig 3.

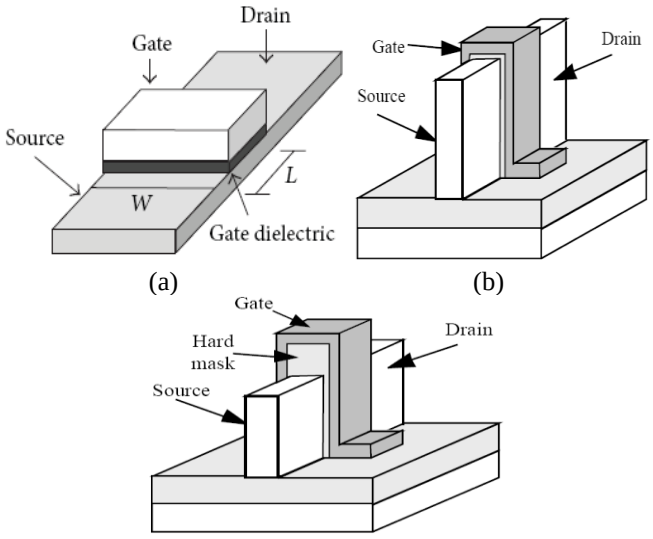


(a) (b)

Fig 3: Structural comparison between a) Bulk and b) SOI MOSFETs

SOI transistors are classified into two types: PDSOI- if the Si film (typically 100nm or more) on the BOX layer is thicker than the depletion region depth beneath the gate oxide and FDSOI if the body thickness is thin enough (typically 50nm or less) or the doping concentration of the body is low enough to be fully depleted. FDSOI transistors have superior advantages over PDSOI transistors in terms of extremely low sub threshold swing, no floating body effects and low threshold variation with temperature. SOI technology provides the corner stone for multi gate transistors [12].

Among multi gate transistors, the foremost to mention is the DELTA MOSFET which is made in a tall and ultra-thin silicon island called "finger", "leg" or "fin" (fig 4b) [13]. This was the first reported FinFET structure in the literature. The FinFET structure is similar to DELTA, except for the presence of a dielectric layer called "hard mask" on top of the silicon fin. The hard mask is used to prevent the formation of parasitic inversion channels as the top corners of the device. While the channel of the planar MOSFET is horizontal (fig 4a), that of FinFET is vertical(fig 4c).



(a) (b) (c)

Fig 4: a) Planar MOSFET ; Double Gate MOSFET structures b) DELTA MOSFET c) FinFET

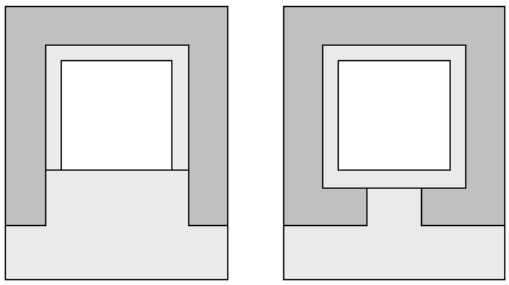
The key parameters in multi-gate FETs are *fin width* which is the thickness of the thin, fully depleted semiconductor body and *fin Height* is the height of the vertical fin. It is worth noting that the minimum feature size in multi-gate transistors is the fin width (H_{fin}) and not the gate length. In FinFETs, H_{fin} determines the channel width. That gives FinFETs, a special property called width quantization which says that effective channel width *Weff* must be a multiple of H_{fin} i.e, widths can be increased by using multiple fins[14-16]. The effective channel width is thus equal to

$$Weff = 2\ n\ H_{fin} \qquad (4)$$

Where n is an integer number that is equal to the number of fins in the device.

The Trigate MOSFETs (TGMOSFETs) have gates on three sides of its channel (fig 6a). The thickness of the dielectric on top of the fin is reduced in TGMOSFETs in order to create the third gate. The thickness of the fin also adds to channel width. Therefore TGMOSFETs enjoy a slight width advantage over FinFETs[17]. They also have less gate source capacitance compared to FinFETs due to the additional current conduction at the top surface but they suffer from additional parasitic resistance as well as increased layout area.

The electrostatic integrity of triple gate MOSFETs can be improved by extending the sidewall portions of the gate electrode to some depth in the buried oxide and underneath the channel region. Under this category the prominent structures are Omega-gate (Ω) FET and PI-gate (π) FET (fig 5) [18, 19]. The π-gate and Ω-gate MOSFETs have an effective number of gates between three and four.



(a) (b)

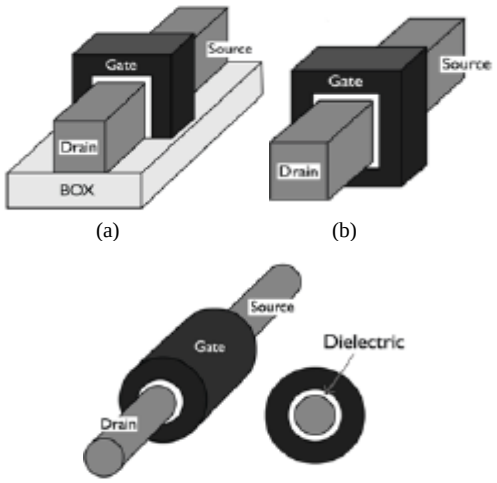
Fig 5: Cross sectional view of a) Ω-gate FET and b) π-gate FET

Ω-gate FET has the closest resemblance to the GAA transistor for excellent scalability, and uses a very compatible manufacturable process similar to that of the FinFET. ΩFET achieves area efficiency by using a tall silicon body. In Pi gate MOSFET, the gate is in the shape of the uppercase Greek letter Pi. The gate extension in the buried oxide shields the back of the channel region from the electric field lines from the drain almost as well as an actual back gate would. The Pi-gate SOI MOSFET can readily be manufactured by extending the sidewalls of the gate material in the buried oxide gives rise to a virtual back gate which effectively enhances current drive and shields the back of the channel region from electric field lines from the drain. As a result, DIBL and subthreshold characteristics comparable to those of a quadruple-gate (or GAA) structure are obtained.

Under quadruple gate structures, GAA FET is the promising structure. It features the gate fully surrounding the channel body and thus providing the best possible electrostatic control (fig 6b). The reduction in channel width and thickness can further increase the effectiveness of the gate control [20]. Therefore, an ultrathin and narrow body (nanowire) MOSFET, when combined with the GAA structure, is deemed to be a major candidate for extreme

CMOS scaling provided the process complexities such as fabrication of short wires and the gate definition under the body are solved. With further gate length reduction, one can expect extremely high drive current from GAA SiNW (Silicon NanoWire) structures (fig 6c)[21]. Besides excellent electrical performance, these devices are immune to substrate bias effects. The gate-all-around MOSFET offers the best gate control but suffers from process complexity and implementation difficulties.

The Inverted T-gate FET (ITFET) is novel device architecture that takes advantage of both vertical and horizontal thin-body devices [22]. An ITFET device comprises of an Ultra-thin body planar horizontal channels and vertical channels in a single device (Fig 7(a)). The devices have multi-gate control around these channels to improve short channel control. A single device has multiple orientations and hence mobility enhancement of both (110) and (100) planes can be used optimally. The structure of ITFET has falling over during processing. It also allows for transistor action in the space between the fins, which is left unused in most of the other MuGFETs. These additional channels increase the current drive. This feature allows various advantages to process, device, circuits and future scaling.

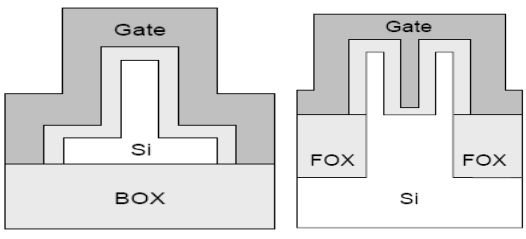


(a) (b)

(c)

Fig 6: SOI MOSFET structures of a)TG FinFET b) Quadraple gate (GAA) c) surrounding gate (GAA) nanowire

The multi-channel FET (McFET) is a modified bulk FinFET structure where a trench is etched in the center of the fin. The trench is filled by growth of gate oxide and the deposition of gate material (Fig 7(b)). This process produces a device having two very thin twin fins running from source to drain[23].



(a) (b)

Fig 7: Cross section of (a) Inverted T-Channel FET and (b) Multiple channel FET

MIGFET devices comprise of gate on two sides of the silicon fin, but the gates can independently control the channel region. MIGFET has been demonstrated to perform dynamic threshold control. Tying the gate and the body of an SO1 MOSFET together, a DTMOS is obtained. Different from the hybrid operating mode (Bipolar and MOSFET), DTMOS threshold voltage drops as the gate voltage is raised [24]. In the meantime, the inversion charge becomes higher and the electric field lower in channel region for DTMOS, resulting in a much higher drive current than a conventional .bulk or SO1 MOSFET. Furthermore, DTMOS has the more ideal subthreshold swing than the conventional MOSFET because of the varied threshold voltage.

Each MGFET has its advantages and challenges. Among them, double gate devices can offer excellent short channel control improved current characteristics with less layout overhead. The FinFET is the most promising of these devices [25]. In the past decade, FinFET technology has been explored by many researchers and has gone through much advancement. In the next section, a close insight on FinFET technology is presented.

V. FINFET TECHNOLOGY

The FinFET technology can fabricate transistors with either a single gate surrounding the silicon fin [3T FinFet, Fig 8(a)], or two gates which can be independently biased [4T FinFET, Fig 8(b)]. 3T FinFETs are also called as SG (Shorted Gate) FinFETs whose front and back gates are physically shorted. Both gates are jointly used to control the electrostatics of the channel[29]. Hence higher on-current and lower I_{off} is produced. The 3T FinFETs or the planar double-gate MOS(DGMOS) transistors with a very thin silicon film can achieve, for sub-100nm gate lengths, a better subthreshold slope S and drain induced barrier lowering (DIBL) with respect to conventional bulk MOSFETs, thus reducing the sub-threshold leakage I_{off}. The 4T FinFETs are also called as IG (Independent Gate) MOSFETs whose front and back gates are physically isolated and can be independently controlled by applying different voltages. However IG FinFETs occupy additional layout area due to need of placing two separate gate contacts [26]-[28].

The 4T-FinGFET enables the threshold voltage of G1 to be raised or lowered by G2 to achieve a higher range of I_{on}/I_{off} performance (Fig 9). This structure is particularly useful in power management, where high I_{on}/I_{off} ratio header and footer transistors are used.

The SG FinFETs can be classified further based on the asymmetries in their device parameters. Symmetric SG FinFETs have same work function for front and back gates where as difference in work function gives asymmetric SG FinFETs (ASGs). ASGs can be fabricated with selective doping of two gate stacks. They have very promising short channel characteristics and reduced I_{off} when compared to SGs. Further depending on the type of asymmetries introduced, different ASGs came into existence. Asymmetric Drain-Source Extended (ADSE) which improves SCEs because of an indirect increase in channel length but there would an increase in layout area.

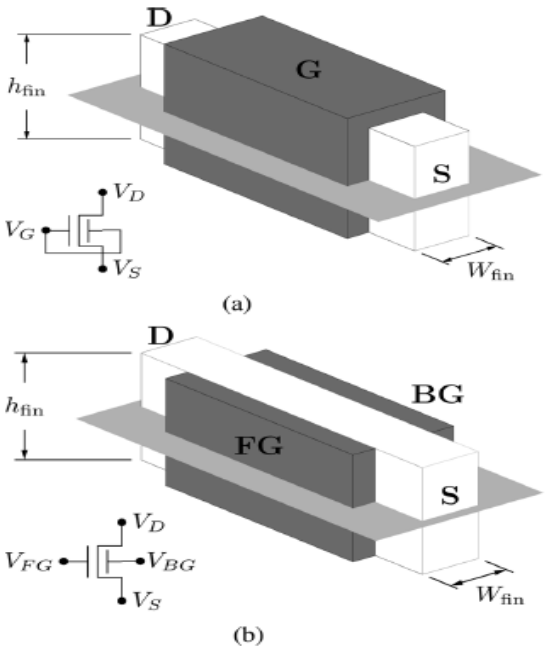


Fig 8: Schematic structure of 3T and 4T FinFets respectively. In the 4T transistor, the gate are separated and can be driven independently (four terminal device) [2] where as in the 3T device both gates are connected as one terminal (three-terminal device). The plane depicted in light gray represents the cut used to obtain the 2-D device which is the one simulated throughput this work. Circuit diagram symbols are shown for (a) 3T FinFET (b) 4T FinFET.

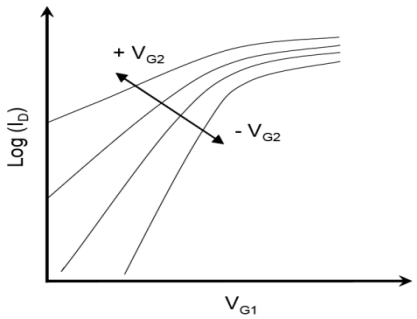


Fig 9: 4T-FinFET drain current as a function of G1 voltage (V_{G1}) and G2 voltage (V_{G2}). V_{G2} affects I_d vs. V_{G1} curves.

Asymmetric drain-source Doped (AD) in which a magnitude difference in drain and source doping concentrations is introduced. SCEs are improved due to lower electric fields in lower doped drain. However, ADSE and AD FETs destroys the interchangeability of source and drain which affects the FinFET's pass transistor characteristics. Asymmetric Oxide Thickness (ATox) provides good sub threshold slope.

FinFET technology leads to performance enhancement and improved variation due to reduction in channel doping concentration. The low channel doping also ensures better mobility of carriers inside the channel which makes FinFET's performance superior to that of planar MOSFETs[31]. Despite of various advantages, FinFETs are facing challenges due to process variations such as side wall roughness (SWR), lithographic limitations, temperature variation and so on. The temperature variation is more severe in SOI FinFETs because oxide layer under the fin has poor thermal conductivity[32]. Hence, heat generated cannot dissipate easily in SOI FinFETs. I_{off} degrades in all FinFETs at higher temperature. Here ASGs are advantageous when compared to SGs.

VI. DIGITAL CIRCUIT DESIGN USING FINFETS

Digital circuit design using FinFETs can be built with the help of n/p FinFETs whose schematic symbols are shown in fig 10.

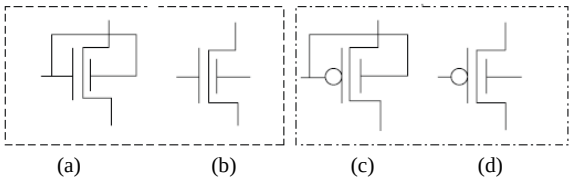


Fig 10: Schematic schematics of a) SG nFinFET b)IG nFinFET c) SG pFinFET d) IG pFinFET

The four possible configurations of inverter using FinFETs have been modeled by Debajit et al. based on SG and IG FinFETs [32]. They are called SG, low-power (LP), IGn and IGp INV (fig 11). Among them, SG INV will have compact layout.

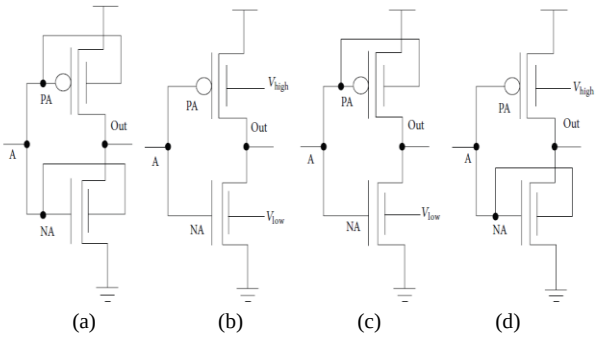


Fig 11: Schematic diagrams of (a) SG INV (b) LP INV (c) IGn INV (d) IGp INV

A number of design opportunities can be explored in FinFETs[33-35] which give scope for optimized delay and power consumption ranging from circuit level to architectural level.

MGFETs can be simulated using the simulation tools such as virtuoso tool from cadence and Sentaurus from Synopsis which allow mixed-mode simulation.

VII. CONCLUSION

The influence of electrostatics of bulk and SOI FETs the channel has been discussed. SOI technology gives promising results in controlling SCEs when compared to bulk MOSFET technology. By reducing the EIF, SCEs can be mitigated. In order to do that gate oxide thickness and depth of depletion has to be reduced. A better control of gate on the channel can be obtained by introducing additional gates in the MOSFET structure which results in multi gate nanoFETs. The characteristics of various types of MGFETs have been discussed. Though an area overhead is introduced by MGFETs, they have advantages in terms of controlled SCEs which in turn fetch in reducing the leakage current through which reduction in power consumption and power dissipation and improved scaling can be achieved.

Among MGFETs, GAA FET provides the best possible electrostatic control on the channel but suffers from implementation difficulties due to process complexity. On the other hand, FinFETs show promising process level control and less overhead on implementation. They are suitable

replacements for planar MOSFETs. 3T circuits have a packing density that is comparable to bulk circuits, whereas 4T circuit suffer from a significant increase in area. In the future, this area overhead could be reduced at the process level by increasing the fin height, although at the expense of an increased minimum channel width (and active power in minimum-sized circuits). Despite the consequent increased interconnect parasitic. FinFET circuits still have a slight advantage in terms of active power, compared to bulk circuits. The Multi bridge channel approach can be applied to nanoFETs for achieving the lowest leakage and the highest energy efficiency.

It is premature to declare a clear winner among multi gate FETs. Possible solutions are still to be explored in different types of nanoFETs to achieve best possible control on device parameters.

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