Distribution system protection using parallel resonance fault current limiter for a three phase system

M.Ramesh, P.Suresh Babu, V Mahendra

***Abstract*— This paper proposes a parallel-*LC*-resonance type fault current limiter (FCL) that uses a resistor in series with a capacitor. The proposed Fault current limiter is capable of limiting the fault current magnitude near to the pre-fault magnitude of distribution feeder current by placing the mentioned resistor in the structure of the FCL. In this way, the voltage of the point of common coupling does not experience considerable sag during the fault. In addition, the proposed FCL did not use a superconducting inductor which has high construction cost. Analytical analysis for this structure is presented in detail, and simulation results using power system computer-aided design/electromagnetic transients, including dc software are obtained to validate the effectiveness of this structure. Also, an experimental setup is provided to show the accuracy of the analytic analyses and simulation results.**

***Index Terms*—FCL, LC Resonance, three phase system.**

I. INTRODUCTION

The growth of power systems and their interconnections has results in increasing the short circuit current level.The most ways to limit high-level fault currents are upgrading switchgear and other equipment, splitting the power system grid, using higher voltage connections (ac or dc), using high impedance transformers, etc. These alternative may create other problems such as power system safety loss, reliability, high cost, and more power losses [1]–[4].

Fault current limiters (FCLs) are developed to overcome the aforementioned problems. An ideal FCL should have the following characteristics [5], [6]:

1) Zero impedance in the normal operation;
2) No power loss in the normal operation;
3) Large impedance in the fault conditions;
4) Quick appearance of impedance when a fault occurs;
5) Fast recovery after fault removal.

The implementation of FCLs in electric power systems is not restricted to suppressing the amplitudes of short-circuit currents. They are also utilized to variety of performances such as power quality improvement, power system transient stability enhancement, reliability improvement, and increasing transfer capacity of system electrical energy. Therefore, an ideal FCL should have another important characteristic in addition to the listed characteristics. It should play the load impedance role and be equal to the load impedance during fault to better operation in such performances [7]–[11].

Different topologies for the FCL are introduced in literatures such as superconducting FCLs (SFCLs), solid-state FCLs, flux-lock-type FCLs, and resonance-type SFCLs. Resonance-type FCLs limit the fault current by using various topologies of series or parallel LC resonant circuits. Series-resonance-type FCLs are composed of a series connection of a capacitor and a superconducting inductor. They do not allow the short-circuit current to increase instantaneously as the fault occurs. However, these FCLs cannot limit the fault current level if the fault continues. Thus, the fault current will increase continually [8-9]. Because of the use of a superconducting inductor, some of these structures need high construction cost. Therefore, they are not commercially available, particularly for third-world countries. On the other hand, resonance-type FCLs, which do not use a superconducting inductor and replace it with an ordinary copper coil, make power losses in their structures.

Previously introduced parallel-resonance-type FCLs have used two anti-parallel semiconductor switches to make resonance condition between L and C. Operation of such structures results in large oscillations on the line current caused by LC resonance at first moments of the fault. These oscillations may harm system equipment [2-3].

In this paper, a new structure for a parallel-LC-resonance type FCL is introduced. The proposed FCL uses a resistor in series with a capacitor, and therefore, it can simulate load impedance during fault. By this way, it can limit the fault current level near to prefault condition. From the power quality point of view, by equating fault current and before-fault line current, the voltage of the point of common coupling (PCC) will not experience considerable change during fault condition, and power quality will improve. In comparison with the previously introduced resonance-type FCLs, this FCL does not use a superconducting inductor in the resonant circuit, and as a result, it is simpler to manufacture and has lower cost. Its inductor is bypassed because of small voltage drop on the diode bridge in the normal operation, and therefore, it has negligible power losses. On the other hand, by using the proposed FCL, the fault current will not increase continually, which happens in most of series-resonance-type FCLs. By using the resistor in this structure, the problem of line current oscillations in the fault condition is solved. Analytical analysis and design considerations for this FCL are

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presented, and matrix laboratory (MATLAB) software is used to solve the resulted formulas. The circuit operation in the normal and fault conditions is simulated by using PSCAD/EMTDC software [5]. Experimental results in laboratory scale are presented too.

II. POWER CIRCUIT TOPOLOGY AND PRINCIPLES OF OPERATION

Fig. 1 shows the single-phase power circuit topology of the proposed FCL. It is necessary to use a similar circuit for each phase in a three-phase distribution system.

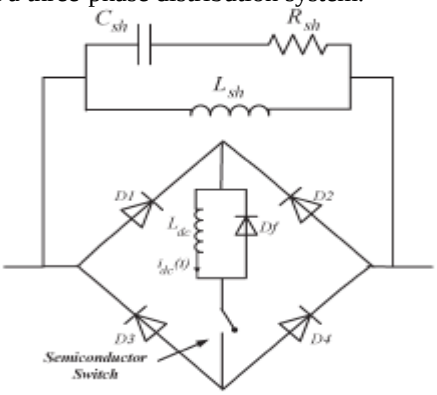

Fig. 1.Single-phase power circuit topology of the proposed parallel resonance type FCL.

This structure is composed of two main parts which are as follows.

1) Bridge part: This part consists of a rectifier bridge containing *D*1–*D*4 diodes, a small dc-limiting reactor (*L*dc),aself turnoff semiconductor switch (such as a gate turnoff thyristor and an insulated-gate bipolar transistor) and its snubber circuit, and a freewheeling diode (*D*f).
2) Resonance part: This part consists of a parallel *LC* resonance circuit (*L*shand *C*sh) (its resonant frequency is equal to power system frequency) and a resistor *R*sh in series with the capacitor.

The bridge part of the proposed FCL operates as a high-speed switch that changes the fault current path to the resonance part when the fault occurs. Obviously, it is possible to substitute this part with an anti parallel connection of two self-turnoff semiconductor switches [2], [3]. Using a diode rectifier bridge has two advantages compared to two anti parallel switches as follows.

1) This structure uses only one controllable semiconductor switch which operates in the dc side instead of two switches that operate in the ac side. The control circuit is simpler because of no need for ON/OFF switching in the normal operation case.
2) It is possible to use a small reactor in series with the semiconductor switch at the dc side. This reactor plays two roles as follows.

a) It is snubber for a semiconductor switch.
b) It is as a current limiter at first moments of fault occurrence

However, placing the dc reactor inside the bridge makes the voltage drop on it because of dc current ripple. However, the current ripple is low, and consequently, the voltage drop caused by it is not considerable in comparison with the feeder's voltage. Current ripple and voltage drop equations are studied completely in [6] and [2]

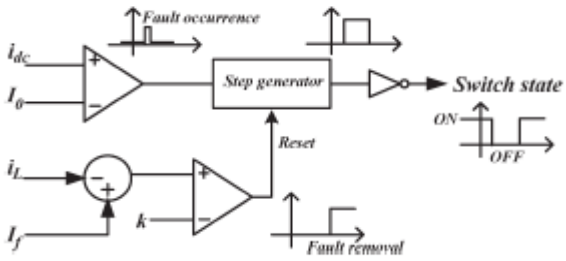

Fig. 2. Control circuit of the proposed FCL

It is important to note that high-rating semiconductor switches are commercially available with current rating up to 24 kA and voltage rating up to 4 kV. Also, it is possible to use some series and/or parallel self-turnoff switches considering high current and voltage levels. The semiconductor switch needs a suitable snubber circuit for its protection, which is not shown in Fig. 1 for simplicity. Also, high-rating semiconductor switches, their protection procedure, and minimization of their power losses are discussed in.

From the power loss point of view, in the normal condition, the proposed FCL has the losses on the rectifier bridge diodes, the semiconductor switch, and the small resistance of the dc reactor. Each diode of the rectifier bridge is ON in half a cycle, while the semiconductor switch is always ON. Therefore, the power losses of this FCL in the normal operation can be calculated as

$$P_{loss}=P_R+P_D+P_{sw}=R_{dc}I^2_{dc}+4V_{DF}I_{ave}+V_{SWF}I_{dc} \quad (1)$$

Where

*I*DC=dc-side current which is equal to the peak of the line current(I_{peak});
R_{dc}=resistance of the dc reactor;
V_{DF}=forward voltage drop on each diode;
*V*SWF =forward voltage drop on the semiconductor switch;
*I*ave=. average current of the diodes in each cycle that is equal to *I*peak/π.

Considering (1) and the small value of the dc reactor in this structure, the total power losses of the proposed Structure become a very small percentage of the feeder's transmitted power.

Fig. 2 shows the control circuit of the proposed FCL. In the normal operation of the power system, the semiconductor switch is ON. Therefore, *L*dcis charged to the peak of the line current and behaves as a short circuit. Using the semiconductor devices (the diodes and semiconductor switch) and the small dc reactor causes a negligible voltage drop on the FCL.

When a fault occurs, the dc current becomes greater than the maximum permissible current *I*0, and the control circuit detects it and turns the semiconductor switch off. Therefore, the bridge retreats from utility. At this moment, the freewheeling diode*D*fturns on and provides free path for discharging the dc reactor. When the bridge turns off, the fault current passes through the parallel resonance part of the FCL. Consequently, large impedance enters to the circuit and prevents the fault current from rising. In the fault condition, the parallel *LC* circuit starts to resonate. In this case, because of resonance, the line current oscillates with large magnitude [2], [3]. These oscillations may lead to damaging system equipment or putting them in stress. However, by placing a resistor (*R*sh) in series with the capacitor, current transients

damp quickly that will be shown in Section V. In addition, by using *R*sh, the voltage drop on *R*sh causes that the voltage across the capacitor is decreased during fault.

When the fault disappeared, while the semiconductor switch is OFF, the parallel part of the FCL will be connected in series with the load impedance. Therefore, the line current will be decreased instantaneously.

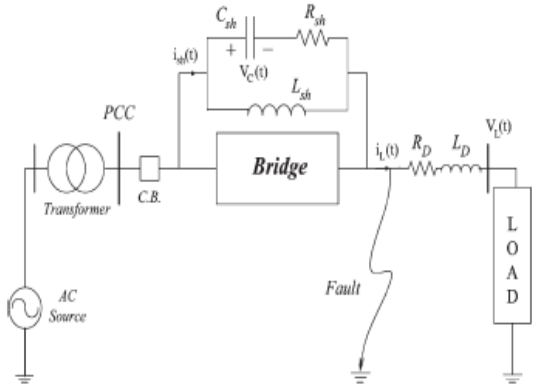

Fig. 3.Single-line diagram of the power system.

To detect this instantaneous reduction of the line current, *i*Lis compared with *If* that can be calculated from

$$I_f = \frac{|\bar{V}_{Pcc}|}{|Z_{eq}|}$$

Where *Z*eqis the equivalent impedance of the resonance part. When the difference of *i*Land *If* becomes greater than *k* as the fault removal sign, the control circuit turns the semiconductor switch on. Therefore, the power system returns to the normal state. The value of *k* can be calculated from

$$K = \frac{|\bar{V}pcc|}{|\bar{Z}eq + \bar{Z}l,\min|}$$

Where *Z*L,min is the minimum impedance of the load on the protected feeder.

As pointed, some of previously proposed FCL structures have ac power losses at the resonant circuit in the normal Condition, because of placing a large inductor in the line current path [8], [9]. However, the proposed structure in this paper has very low losses in the normal condition, because the inductor is bypassed by the bridge part. Also, by choosing proper values for the resonant circuit, the proposed FCL limits the fault current in a way that the power system is not affected by the fault. In such condition, there will not be any considerable voltage sag on the PCC voltage.

III. ANALYTICAL ANALYSIS

Fig. 3 shows the single-line diagram of the power system including the proposed FCL. This figure is composed of a power source, a transformer, a circuit breaker (C.B.), an FCL, a line impedance, and a load. The circuit breaker (C.B.) which is rated for the full system short-circuit current is placed to ensure the adequate protection of the power system during permanent faults. The utility voltage is a three-phase sinusoidal waveform. The utility-side impedance is modeled by a series connection of a resistor *R*s and an inductor *L*s. The analytical analysis is discussed in two modes as follows:

Mode 1) prefault steady-state operation (until *tf* in Fig. 4);

Mode 2) between fault occurrence and fault removal (from *tf*to fault removal time in Fig. 4)

Mode 1

In the normal operation of the power system, the bridge part bypasses the resonant circuit. In this condition, the line current(*iL*) can be expressed by the following differential equation

$$Vs\sin(\omega t) = Ri_L + \omega L\left(\frac{di}{d\omega t}\right)$$

Where

*V*speak of the utility voltage;

ω =angular frequency of the utility voltage;

R = *R*s+ *R*L + *R*D resistance of the source side, load, and distribution feeder;

L = *L*s+ *L*L + *L*D inductance of the source side, load, and distribution feeder.

Therefore, the line current equation can be derived as follows,

$$i_L(\omega t) = \left(\frac{V_s}{\sqrt{R^2+\omega^2L^2}}\right)\left[\left(\frac{L\omega}{\sqrt{R^2+\omega^2L^2}}\right)e^{-\left(\frac{R}{\omega L}\right)\omega t} + \sin(\omega t - \varphi)\right] \quad (5)$$

Where$\varphi = \arctan\left(\frac{\omega L}{R}\right)$

Mode 2

When a short circuit occurs, the dc-limiting reactor can limit the increasing rate of the fault current. The semiconductor switch does not operate until the line current reaches to a predefined value. By semiconductor switch operation in the *t*sw instant (Fig. 4), the bridge is switched off, and the fault current is suppressed by the resonant circuit. Therefore, the differential equation of the fault current can be expressed as follows:

$$L_{sh}L_sC_{sh}\left(\frac{d^3i_L}{dt^3}\right) + \left(R_sL_{sh}C_{sh} + L_sR_{sh}C_{sh} + C_{sh}R_{sh}L_{sh}\right)\left(\frac{d^2i_L}{dt^2}\right) + \left(L_s + R_{sh}C_{sh}R_s + L_{sh}\right)\left(\frac{di_L}{dt}\right) + R_si_L = \left(V_s - L_{sh}C_{sh}\omega^2\right)\sin(\omega t) + R_{sh}C_{sh}V_s\omega\cos(\omega t) \quad (7)$$

with initial values given in (8), shown at the bottom of the page, where *I*0 is the predefined line current for semiconductor switch operation.Equation (7) is solved by MATLAB software, and its results are presented in Section V in detail. After damping transients, the fault current equation can be expressed by

$$i_L = A\cos(\omega t) + B\sin(\omega t)$$

where

$$A = \frac{V_s[R_{sh}C_{sh}\omega(d'-b'\omega^2) - (1-L_{sh}C_{sh}\omega^2) - (1-L_{sh}C_{sh}\omega^2)(c'\omega - a'\omega^3)]}{(C'\omega - a'\omega^3)^2 + (d'-b'\omega^2)^2}$$

$$B = \frac{V_s[R_{sh}C_{sh}\omega(a'\omega^3 - c'\omega) - (1-L_{sh}C_{sh}\omega^2)(d'-b'\omega^2]}{(C'\omega - a'\omega^3)^2 + (d'-b'\omega^2)^2}$$

$$a' = L_sL_{sh}C_{sh}$$
$$b' = R_sL_{sh}C_{sh} + L_sR_{sh}C_{sh} + L_{sh}R_{sh}C_{sh}$$
$$c' = L_s + L_{sh}C_{sh}R_s + L_{sh}$$
$$d' = R_s$$

By considering (9) and choosing proper values for *L*sh, *C*sh, and *R*sh, it is possible to limit the line current in the fault condition in a way that its value is near to the prefault line current. In this case, if the fault occurs, the PCC voltage will not sense the fault.

IV. DESIGN CONSIDERATIONS

As discussed in Section II, Ldc is used to limit the increasing speed of the fault current and help the semiconductor switch to turn off in a safe condition. Therefore, its value can be chosen by considering the current characteristics of the semiconductor switch. For resonant circuit design, two main cases should be taken into account: The first one is equating the resonance part

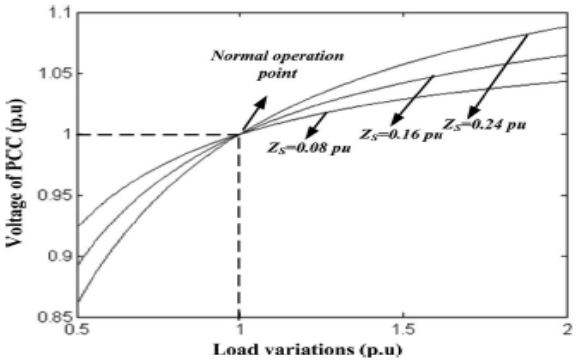

Fig. 4. Voltage magnitude of PCC when the equivalent impedance of the resonance part is not equal to the protected feeder load impedance (non ideal case).

equivalent impedance with the load impedance; the second is the generated heat in the resistor of the resonance part during fault and its design problem. The equivalent impedance of the resonance part Zeq can be derived as follows:

$$Z_{eq} = (R_{sh} - j/\omega C_{sh})//j\omega L_{sh} = L_{sh}/C_{sh}R_{sh} + j\omega L_s \quad (11)$$

For equating this impedance with the load Impedance, Lsh should be equal to the load inductance. The corresponding capacitor value Csh can be calculated considering the resonance condition between it and Lsh. Finally, the resistor value should be chosen in a way that Lsh/Csh$R$sh is equal to the load resistance. However, it is difficult to equate these impedances exactly, and it is an ideal case because of load variation on distribution feeders. From a practical point of view, the parameters of the resonance part can be determined by using the history of measurements of the load at protected feeder and discussed calculations. The following discussion deals with the operation of the proposed structure in practical condition. Fig. 4 shows the magnitude of the voltage deviation of the PCC of the test system from its base value (which is the prefault voltage magnitude of the PCC). The horizontal axis in this figure shows the magnitude of the impedance of the load in per unit where the base value is its impedance of the ideal case. The dashed line shows the existence of the ideal case. The parameter in this figure is the magnitude of the source impedance. This figure shows that, for a wide range of load magnitude variations (0.5–2 p.u. with fixed resonance part parameters), the voltage

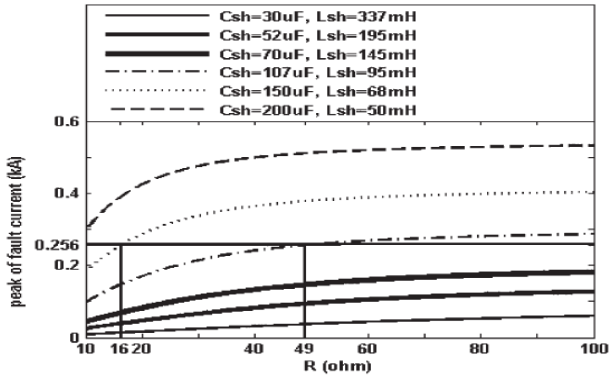

Fig. 5.Variation of the fault current magnitude with respect to Rsh.

magnitude of the PCC for post fault condition changes in an acceptable range, particularly for low values of $|Zs|$.

For considering the generated heat in the resistance of the resonance part, it is possible to change the values of Lsh, Csh, and Rsh and decrease the real part of (11). Note that the magnitude of Zeq should be kept constant. Fig. 6 shows the fault current magnitude with respect to Rsh. The parameter in this figure is resonant LC. The lower limit of Rshis selected to ensure proper transient response of the resonant circuit. The standard values for Csh are obtained from [3], and Lshis calculated by considering the resonance condition between it and Csh in power frequency.

As a numerical example, it is considered that the feeder's average current is 256 A. In this condition, the predesired value of the fault current (256 A) can be achieved by two values for resonant circuit parameters as follows.

Case 1) Csh= 150 μF, Lsh= 68 mH, and Rsh= 16Ω.

Case 2) Csh= 107 μF, Lsh= 95 mH, and Rsh= 49Ω.

$|Z$eq$|$'s in cases 1 and 2 are equal. However, in case 2, the real part of Zeq is smaller than its value in case 1. therefore, the generated heat in Rsh is reduced in fault condition. As a result, the design of Rsh becomes simpler from a thermal point of view.

V. SIMULATION RESULTS

The power circuit topology in Fig. 3 is used for simulation in the fault condition. The simulation parameters are shown in Table I. The fault starts at 1 s and continues to 1.12 s (six cycles of power frequency).

TABLE I
SIMULATION SYSTEM PARAMETERS

Source side data	Power source	20KV,50HZ, $Z_{source} = 0.57 + j\omega 0.003\Omega$
	transformer	20KV/6.6KV,10MVA,0.1 p.u
FCL data	Dc side	$L_{dc} = 0.01\text{H}, V_{DF} = 3V, V_{SW} = 3V, I_0 = 0.5kA$
	Resonance part	$L_{sh} = 0.068H, C_{sh} = 150\mu F, R_{sh} = 16\Omega$
Load side data	$Z_{line} = 0.5\Omega, Z_{load} = 15 + j0.1\Omega$	

when the fault current reaches to I0 that is the predefined fault level, the semiconductor switch turns off, and the line current is limited in the fault condition.Therefore, it is necessary to set the secondary switching device for full short-circuit current of the power system.

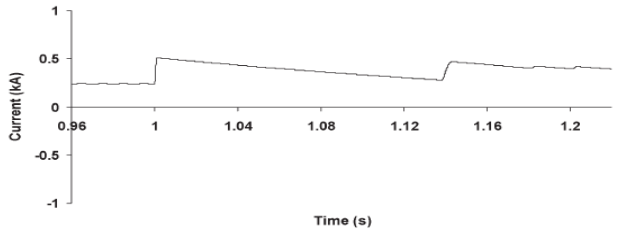

Fig. 7. DC reactor current $I_{dc}(t)$ for the A phase.

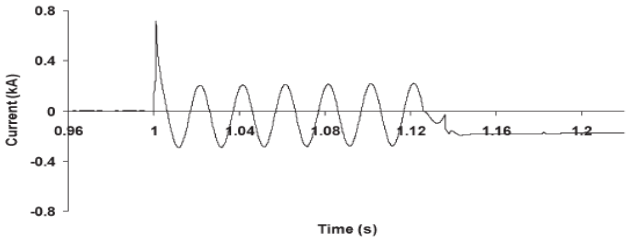

Fig. 8. Resonance part current during the fault *i*sh(*t*) for the A phase

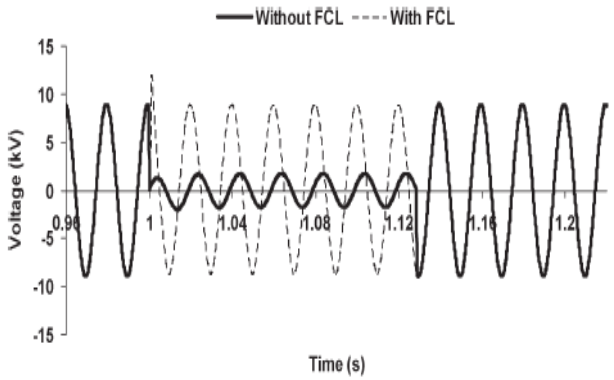

Fig. 9. PCC voltage of the A phase without and with the proposed FCL.

Fig. 7 shows the dc reactor current. As the fault occurs, it starts to charge until semiconductor switch turning-off. After semiconductor switch turning-off, the freewheeling diode turns on and discharges *L*dc. After fault removal, *L*dc recharges because of resonant circuit voltage. By discharging the resonant circuit, the dc reactor current discharges and returns to the normal state.

The current of the resonance part during the fault *i*sh(*t*) for the A phase is shown in Fig. 8. It is obvious that, aftersemiconductor switch operation, the line current will be equal to the resonance part current. Fig. 9 shows the PCC voltage with and without using the proposed structure. As shown in this figure, the proposed FCL can prevent voltage sag on PCC properly. Also, the PCC voltage without using *R*sh in the proposed FCL is shown in Fig. 11.

It is observed that undesired distortions appear on the PCC voltage caused by the resonance current. The capacitor voltage is shown in Fig. 12 To demonstrate the accuracy of the calculations, differential equation (7) that shows the line current during fault is solved by MATLAB software, and its result is shown in Fig. 13. This figure is in good agreement with Fig. 7(c). The peak value of the current in both figures [Figs. 7(c) and 13] is 256 A. The values and variation of the curve show that the results of the calculations are adapted by the simulation result of the PSCAD/EMTDC software. This can prove the correction of (7)–(10).

To study the non-ideal case which is discussed in Section IV, the load is changed to 0.5 p.u. in the simulation system, and its results are shown in Figs. 14 and 15. Fig. 14 shows the line current (A phase) for the nonideal case. As shown in this figure, the line current is smaller than its value during fault. The PCC voltage in such condition is shown in Fig. 15. According to this figure, small voltage sag appears in PCC. This voltage sag is predictable considering Fig. 5.

To determine the rating of the FCL components, it is possible to use the simulation results as well as the design considerations mentioned in Section IV. Of course, for all semiconductor devices, the maximum ON-state current is the peak of the line current. The maximum OFF-state voltage for these devices is the PCC voltage during the fault. The current rating of *L*dc is the peak of the line current. Also, the resonance part inductance *L*sh will appear during the fault. Therefore, in the worst condition,

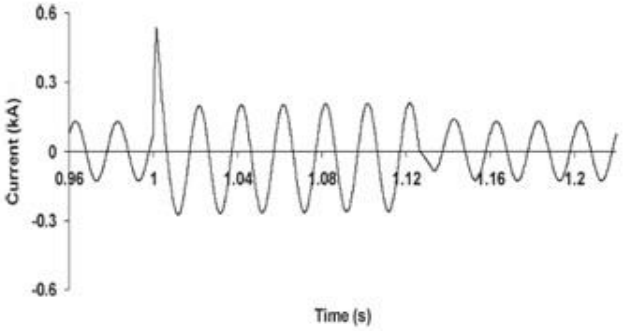

Fig.10: Line current of the A phase in the nonideal case.

its voltage will be the PCC voltage. Thus, its current rating can be determined. For the capacitor *C*sh, a simple voltage-dividing method can be used between it and the resistor *R*sh.

TABLE 2 EXPERIMENTAL SYSTEM PARAMETERS

Source side data	Power source	220 V(peak),50Hz, Z_{source}=0.5+j ω0.005Ω
	transformer	220V/110V,10kVA, 0.1 p.u
FCL data	Dc side	L_{dc}=0.01 H, V_{DF}=1V,V_{SW}=1V,I_o=8A
	Resonance part	L_{sh}=0.07H, C_{sh}=150μF,R_{sh}=15Ω
	Control circuit	Current sensor:CSNE151-100 Gate driver:IR2113 Microcontroller:ATMEGA32 Switch:GW40NC60V
Load side Data	$Z_{line} = 0.5\Omega, Z_{load} = 10 + j25\Omega$	

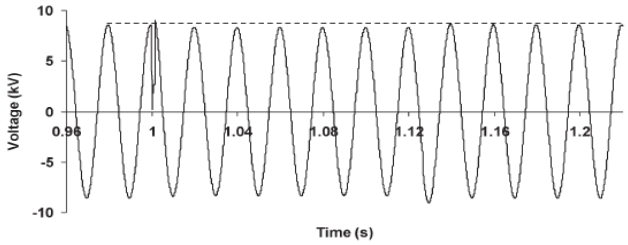

Fig. 11. PCC voltage of the A phase during the fault in the nonideal case

VI. EXPERIMENTAL SETUP

The performance of the proposed FCL is experimentally investigated using a laboratory-scale power system simulator. The power system for the experimental study is shown in Fig. 3. Note that the control circuit of the proposed FCL is implemented by software. The experimental setup parameters and the control circuit data are presented in Table II. According to the available element values in the market and experimental setup facilities, the component values in the experimental setup are selected as much as possible near to the simulation values which were obtained by the proposed design procedure. Fig. 13 shows the line current by using the proposed FCL. This figure is in good agreement with Fig. 7(c). The resonance part current during fault is shown in Fig. 14.

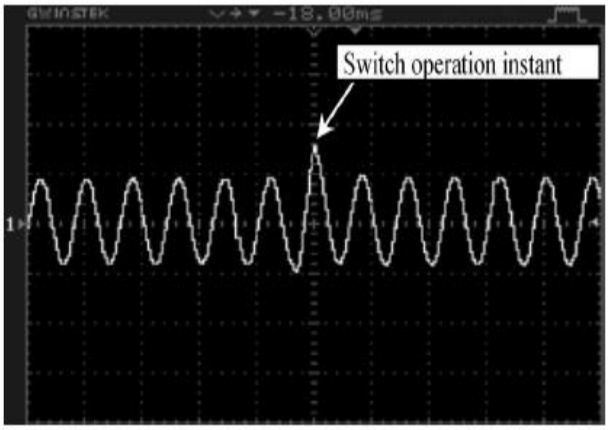

Fig. 12. Line current by using the proposed FCL (current/div.: 5 A; time/div.: 25 ms).

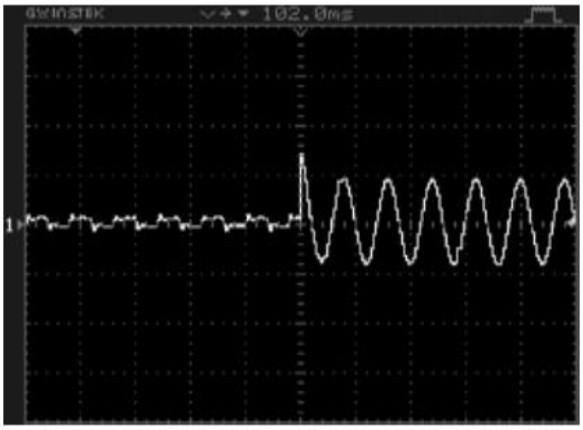

Fig. 13. Current of the resonance part during fault (current/div.: 5 A; time/div.: 25 ms).

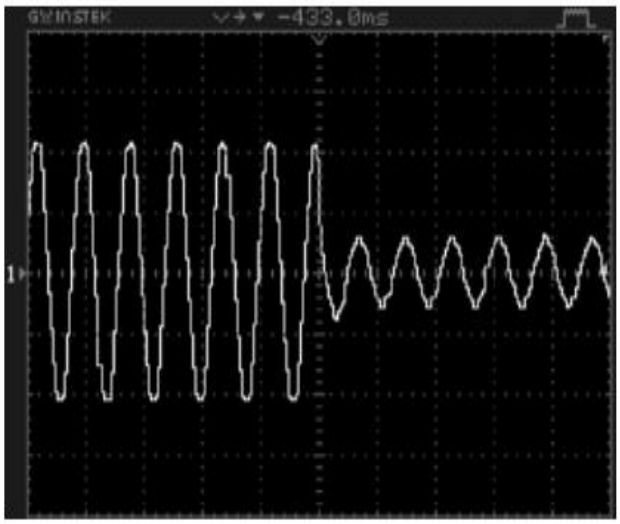

Fig. 14. PCC voltage without using the FCL (voltage/div.: 50 V; time/div.:25 ms).

The PCC voltage without using the proposed FCL is shown in Fig. 13. It is observed that the PCC voltage drops strongly. Using the proposed FCL prevents this voltage sag, as shown in Fig. 14. In such condition, a negligible distortion appears on the PCC voltage at the fault occurrence instant. Notice that the time scale in Fig. 13 is magnified to emphasize the small distortion of the voltage in the fault instant. Figs. 16 and 19 are in accordance with Fig. 7. Fig. 9a shows the capacitor voltagein the fault condition. It is in agreement with Fig. 12.

VII. CONCLUSION

In this paper, a new topology of parallel-*LC*-resonance-type FCL that includes a series resistor with the capacitor of the *LC* circuit has been introduced. The analytical analysis and design considerations for this structure have been presented. The overall operation of the mentioned FCL in normal and fault conditions has been studied in detail. Also, the simulation and experimental results have been involved to validate the analytic analyses. All previously proposed FCLs have goodcurrent-limiting characteristics.

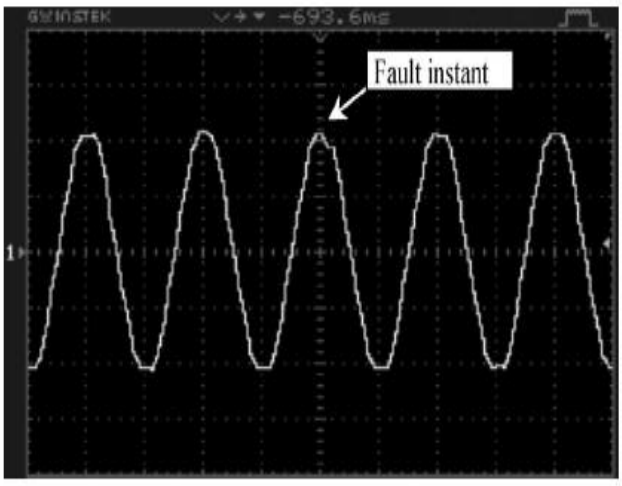

Fig. 15. PCC voltage by the proposed FCL (voltage/div.: 50 V; time/div.: 10 ms).

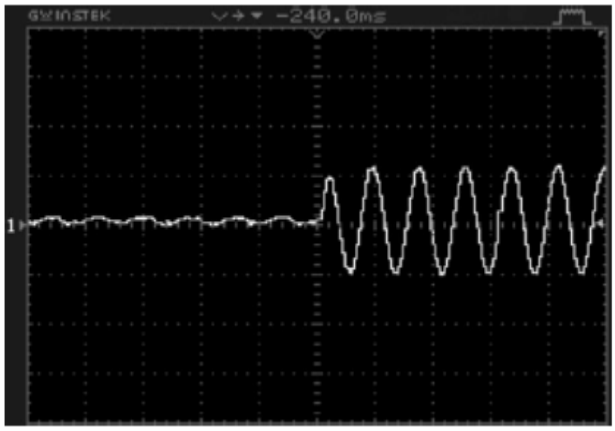

Fig. 16. Capacitor voltage during fault (voltage/div.: 50 V; time/div.: 25 ms)

However, as shown in this paper, the proposed structure can improve the power quality of the distribution system in addition to fault current limiting. The proposed resonance-type FCL can limit the fault current in a way that the PCC voltage does not face considerable sag during fault. This means that, in case of transient faults, it is not necessary to open the line by a circuit breaker. By using R_{sh} in the proposed topology, the transient state after fault damps quickly. In addition, it is capable of controlling the fault current at constant value that is not possible in common series resonancetype FCLs.

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