Smart Reliable Network on Chip and its Area reduction using Elastic buffer

Meera P Alias, Melvin C Jose

***Abstract*— Network on Chip (NoC) is one of the efficient on-chip communication architecture for System on Chip (SoC) where a large number of computational and storage blocks are integrated on a single chip.NoC has more flexibility and reusability when compared with dedicated wires where number of wires increases dramatically as the number of cores grows.In this project 2X2 and 4X4 mesh topology NoC has to be designed and implemented. The proposed NoC is based on adaptive XY routing algorithm. In Adaptive XY algorithm ,if any neighbouring router becomes faulty,faulty link of the router will be bypassed.The area requirements of the NoC is very high.In order to reduce the area,the input and output buffers of the NoC will be replaced with elastic buffers.Inorder to further improve the performance of the NoC ,an arbiter can be introduced.Arbiter is used when many input ports request the same output port and in such cases a priority will be assigned for input ports when they request the same output port. The NoC's performance have to be evaluated and implemented on Spartan3E field programmable gate array kit.**

***Index Terms*— EB,FIFO,NoC,PE,SEC-DED,SoC**

I. INTRODUCTION

Integrating a NoC into the SoC provides an effective means to interconnect several processor elements (PEs) or intellectual properties (IP) (processors, memory controllers, etc.). The NoC medium features a high level of modularity, flexibility, and throughput. A NoC comprises routers and interconnections allowing communication between the PEs and/or IPs. The NoC relies on data packet exchange. The path for a data packet between a source and a destination through the routers is defined by the routing algorithm.

In this paper a new reliable dynamic NoC is being presented[1]. The proposed NoC is based on mesh structure of routers which is able to detect routing errors using adaptive XY algorithm. Data packet error detection and correction is possible as the packet is transmitted between routers.Hamming Error Correction Code applied at the input and output of the router will enable Single Error Correction and Double Error Detection(SEC-DED).

A 2x2 and 4x4 mesh Topology NoC is used in this paper.NoC using First in first out (FIFO) for storage of incoming data in the input and output buffers when replaced with Elastic buffer can reduce the area requirements of the NoC. Arbiters when introduced into NoC can improve the performance when more than one input ports of a router request the same output port.Arbiters assigns priority for each input port when they request the same output port,thereby deciding which input port gains control over the output port first.

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II. LITERATURE REVIEW

Network on chip act as a solution to implement future on-chip interconnection architecture.A typical NoC consists of switches to route the data packets, interfaces to connect each core to a switch in a NoC, and interconnections among the switches as shown in Fig. 2.1. The wires connecting the routers are unidirectional ,so a connection between neighboring routers uses two wires.The Switching Techniques in a NoC is of two types:Circuit Switching and Packet Switching.In Packet Switching entire message is divided into packets and transmitted wheras in Circuit Switching a link is being established before messages are transmitted.

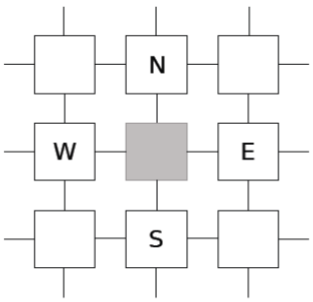


Fig 2.1 Neighbours of a router

2.1.Topology

The topology of NoC depends upon the placement and interconnection of NoC nodes[2]. The ideal characteristics that a NoC provides are low latency, more throughput and less power consumption, less routing area and less complexity.Its difficult to have all these features in a single NoC , so a trade off exists between these features.The topology of the NoC classified as regular and irregular. Mesh and Torus are regular forms of topologies as shown in Fig.2.2.A mesh topology NoC is used here as it is much suitable for a 2D layout and faults can be easily detected.Torus topology is similar to mesh topology except that ends of the row and column are connected.Irregular topology is obtained by mixing different forms and it forms a hybrid ,asymmetric or hierarchical fashion.

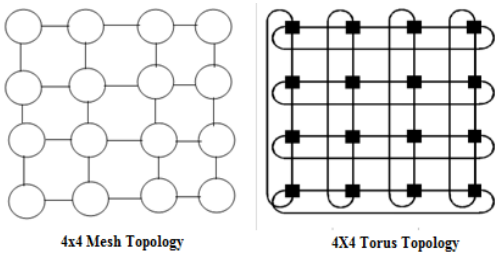


Fig 2.2 Topolgy of NoC

2.2 Routing Algorithms in a NoC

The routing algorithm which defines the path taken by a packet between the source and the destination affects the the efficiency of the communication of NoC.
Routing algorithm can be classified in different ways :-
(i)Depending upon degree of adaptiveness of routing algorithm as adaptive and deterministic routing algorithm
(ii)Depending upon number of destination as unicast and multicast routing algorithm
(iii) Depending upon routing decisions as source routing,distributed routing,centralized routing and multi phase routing etc..

2.2.1 XY Routing Algorithm

There are different types of XY Routing algorithms[3].XY Routing Algorithm is an example of deterministic routing algorithm.It takes a fixed path between the source and destination.In XY Routing Algorithm,routing first takes place in x direction and then in y direction.An adaptive XY algorithm is used here which bypasses the faulty router and reaches the destination by using XY algorithm.

2.3 Hamming code Error Correction

In communication system, a secure data transmission from transmitter to receiver is very major issue for error free transmission.There are number of methods.One of them is Hamming code method[4].The central concept in detecting or correcting errors is redundancy. Inorder to detect or correct errors, some extra bits are appended with the data. These redundant bits are added by the sender and removed by the receiver at positions in power of 2.Their presence allows the receiver to detect or correct corrupted bits. The (n, k, t) code refers to an 'n'-bit code word having 'k' data bits (where n > k) and 'r' (=n–k) error-control bits called 'redundant' or 'redundancy' bits with the code having the capability of correcting 't' bits in the error (i.e., 't' corrupted bits).If the total number of bits in a transmittable unit (i.e., code word) is 'n' (=k+r), 'r' must be able to indicate at least 'n+1' (=k+r+1) different states. Of these, one state means no error, and 'n' states indicate the location of an error in each of the 'n' positions. So 'n+1' states must be discoverable by 'r' bits; and 'r' bits can indicate 2^r different states. Therefore, 2^r must be equal to or greater than 'n+1'i.e $2^r \geq n+1$ or $2^r \geq k + r + 1$ The value of 'r' can be determined by substituting the value of 'k' (the original length of the data to be transmitted).For example, if the value of 'k' is '7,' the smallest 'r' value that can satisfy this constraint is '4'i.e

$$2^4 \geq 7+4+1 \qquad (1)$$

In this paper ,18 bit data is converted into a 24 bit packet and transmitted.The redundant bits are positioned as shown in Fig.2.3 below and their calculation is shown in Fig.2.4 respectively.

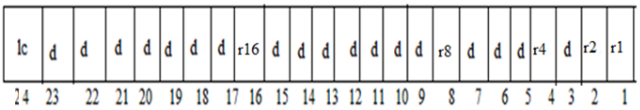


Fig 2.3 Position of redundancy bits in (18,6,1) Hamming code

To construct a single error correcting plus double error detecting code,one more position "lc "is added for checking all the previous positions,using an even parity check.

r	Even parity of bit positons
r1	1,3,5,7,9,11,13,15,17,19,21,23
r2	2,3,6,7,10,11,14,15,18,19,22,23
r4	4,5,6,7,12,13,,14,15,20,21,22,23
r8	8,9,10,11,12,13,14,15
r16	23,22,21,20,19,18,17,16
lc	1 to 23

Fig 2.4 Calculation of redundancy bits in Hamming code

Three different cases exists under this condition.

- No errors:All parity checks including the last are satisfied
- Single error:The last parity check fails in all such situations whether the error be in the information,the orginal check positions or the last check position.The orginal checking number gives the position of error,where zero value means the last check position
- Two errors:In all such situations the last parity check is satisfied and the checking number indicates some kind of error

III. PROJECT OVERVIEW

The RKT-NoC is a packet switched network based on intelligent independent reliable routers called RKT switches. The architecture of the RKT switch is shown in Figure 3.1. The RKT-switch is characterized by its architecture having four directions (North, South, East,West) suitable for a 2-D mesh NoC. The PEs and IPs can be connected directly to any side of a router. Therefore, there is no specific connection port for a PE or IP.In the four port router shown in Figure 3.1,An IP can replace several input ports and can be thus strongly connected in the network.
A 2X2 and 4X4 mesh topology NoC is used in this project.The single switch structure is being replicated to form a mesh topology.The overall architecture of the RKT switch is as follows.

- Firstly,the packet enters the router through the loopback module.Single bit Errors if any in the received packet is corrected by Hamming ECC.If there is more than two errors in the received packet,that packet will be discarded.
- The decoded packet will be stored in the input buffer of received input port

- The same decoded packet will also be stored in the output buffer of the other ports.
  The output buffer which will get enabled is decided by the adaptive XY algorithm.XY algorithm is such that it first routes in x direction and then in y direction.If there exists any error in any port of the router ,that particular port will not get transversed.The
  packet will transverse through some other port of the same router.
- The output buffer which was enabled will get encoded using Hamming ECC.
- The encoded packet will be out of the router module through the dataout of the loopback module.This packet will act as input to other router module.
- A centralized journal is maintained that states a particular port is faulty,when threshold of number of errors in the journal reaches three.

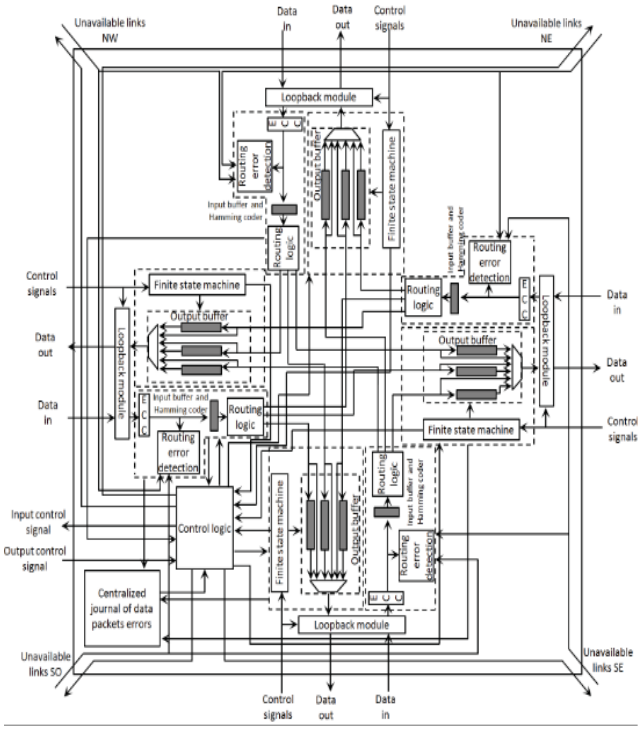


Fig 3.1 Architecture of the reliable router

A loopback module is implemented in each of the four ports of the router, as illustrated in Fig 3.1.The packet enters and leaves the router through the loopback module. The architecture of the loopback module is depicted in Figure 3.2. The logic control block checks the availability of the neighboring router in order to transmit the data packets (data_request_in signal). If no loopback is required, a semi-crossbar connects the buffer to the data_out signal in order to send the data packets the data packet on the data_loopback bus. When loopback is required as neighbouring link is unavailable, the data packet is looped back inside the router and will be considered as a new packet.Thus by loopbacking the same packet will be transversed through some other port of the same router.
In the structure of the RKT switch shown below,an arbiter is also introduced.An arbiter assigns priority for a router when more than one input ports of a router request the same output port.The arbiter thus introduced removes the contention problem.

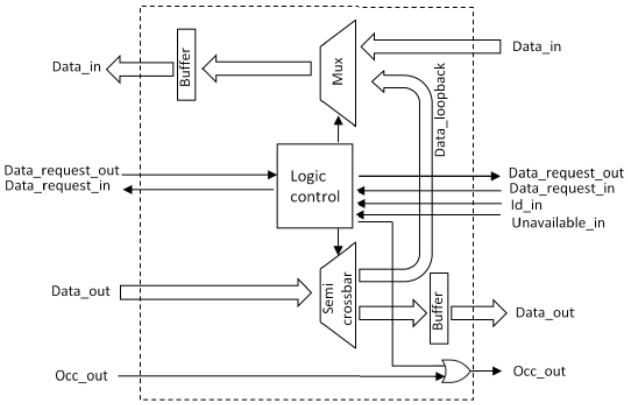


Fig 3.2 Architecture of Loopback module

3.1 Arbiter

Many input ports will be requesting to access a common physical channel resource. In this case, an arbiter is required.If many flits arrive at buffers from several channels and these flits are destined for one physical channel, an arbiter receives request signals from buffer.The role of arbiter is shown in Fig 3.3 where it receives requests from north,east,west input ports for south output port. A priority is assigned for each input port for a particular output port.For the south output port shown in Fig 3.3 ,the order of priority is west input port followed by east input port and north input port.

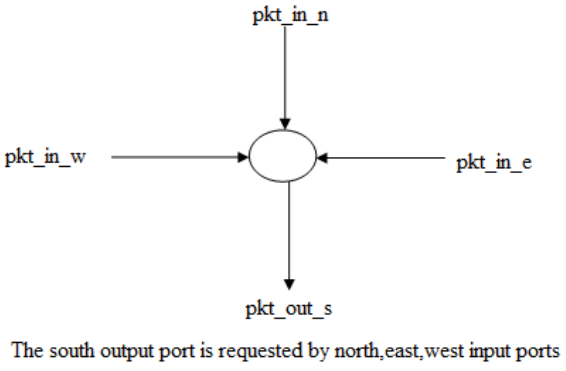


Fig 3.3 Role of arbiter

3.2 Elastic Buffer

Buffers are commonly implemented in network routers and used by the flow control scheme to enqueue contenting packets or flits . Buffers occupy almost 75 percent of the network area.So there is a need to eliminate these buffers in order to reduce area and power consumption. Elastic buffer (EB) flow control is proposed to eliminate router buffers while preserving buffering in the network[5].Pipeline flip-flop (FFs) become EBs with two storage locations is obtained through the addition of a small logic block which controls their master and slave latch enable inputs independently as shown in Fig.3.4 respectively. The two inputs are still gated by the clock as in a normal master-slave FFs.Master Flip flop is gated by write signal and slave signal is gated by read signal. Having EBs in sequence enables channels to act as distributed FIFOs. Flits progress among EBs using a ready-valid handshake .Thus inorder to reduce the associated area and energy costs buffers based on FIFOs are replaced with Elastic buffer in this paper.

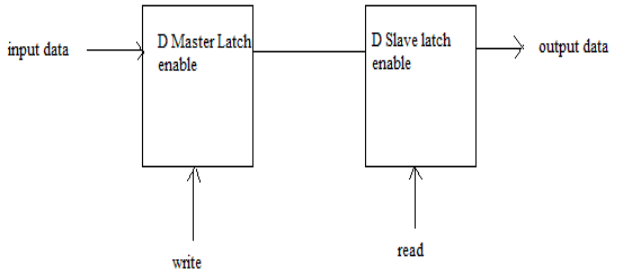


Fig 3.4 Architecture of Elastic Buffer

IV. RESULTS

The NoC topology for 2x2 mesh size is shown in Fig 4.1 below.Four routers are connected to each other so as to form a mesh structure.The input can be connected to any of the router.Each router has x and y co-ordinate associated with it which is represented inside the node.

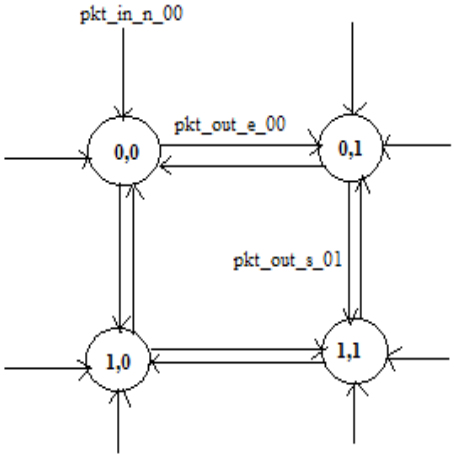


Fig 4.1 A 2X2 Mesh Topology NoC

Suppose that packet is entered through the north port of the router(0,0).The destination is towards the router (1,1).The packet will be out through the east port of router (0,0) which is the west input port of the router(0,1).Single bit error will be corrected and transmitted out of east port of router (0,0).This packet act as input to west port of router (0,1) and will be out through the south port of router (0,1).When the packet reaches destination ,the local request will be made high.The output waveform shown in Fig 4.2

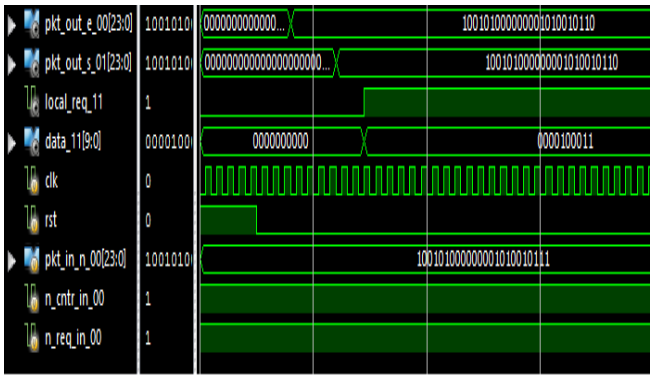


Figure 4.2 Output waveform for 2x2 mesh topology

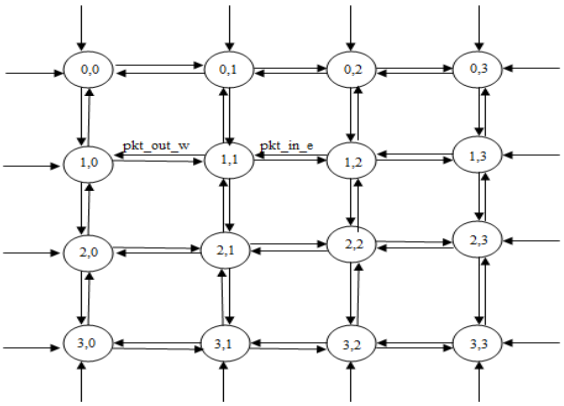


Figure 4.3 A 4x4 mesh topology for routing error detection

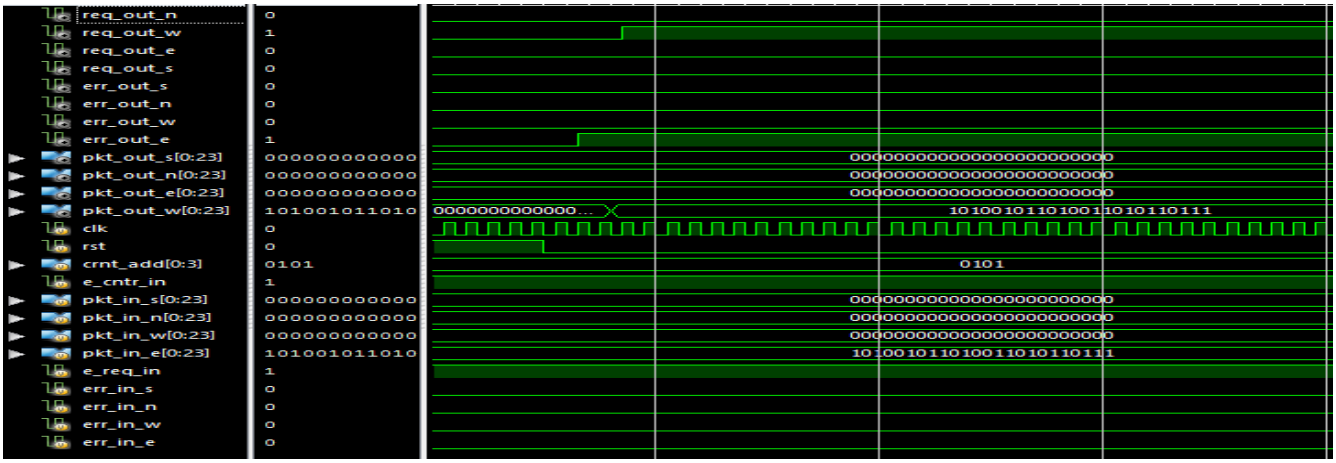
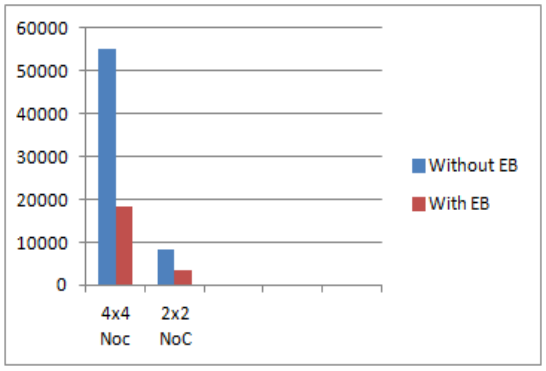


Figure 4.4 Output waveform for 4x4 mesh topology for routing error detection

A 4X4 mesh topology NoC with error in the east port of router (1,1) is shown in Figure 4.3.The output waveform for the above 4X4 mesh topology NoC is shown in Figure 4.4.The current address of the router is (1,1) as shown by "crnt_add" in Figure 4.4.The 24 bit packet24'101001011010011010110111 enters through the east.port of the router (1,1) given by "pkt_in_e".The Hamming decoder decodes the packet and finds the destination of packet towards the router (2,1).The router (1,1) checks the availability of the links in north,south,west,east directions given by "err_in_n", "err_in_s" "err_in_w" "err_in_e".All the links are available as all of them are

0.According to XY algorithm packet should be transmitted out through south port of router (1,1) but the packet is transmitted out through the west port of router (1,1) making "req_out_w" high instead of "req_out_s" .This creates a routing error given by east port of router (1,1) making "err_out_e" high.

Table 4.1 Comparison of area of 2X2 NoC and 4x4 NoC with and without elastic buffer



The Table shown in Table 4.1 shows the comparison of area of 2x2 and 4x4 NoC with and with out Elastic buffers.There is a significant reduction in the number of LUTs when buffers using FIFOs are being replaced with Elastic buffers.

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