Design and Optimization of a Low DC Offset in Implanted System for ENG Recording Based on Velocity Selectivity Method

Assad I. K. Al-Shueli

***Abstract*— The major target of this paper is the design of advance signal processing system based on minimized length of bits required for digital-to-analogy converter (DAC) for velocity selectivity recording (VSR) approach. The main application of this device is peripheral nerves recording (*electroneurogram*-ENG) by exploring a spectral analysis for the propagation of neural activities in the *velocity* domain recording using VSR in implantable application. This research adapted a flexible, compact, and energy efficient dc offset removal circuit. An optimization design has been used based on best possible process involving linearity and area is thus suggested. The system process acquired using this approach were characterized as having a 10-bit signal processing for DAC resolution, with 1.4 mA rms output current, with minimum size around 0.02 mm^2 of chip area, using FPGA board as prototype design. This paper also explores the design temperature vibration in online recording; minimization the output DC offset decrease the heat emission which is significantly for long term implementation applications. This study proposed an analysis circuit configuration demonstrate that this approach could achieve a small DC offset error, with small size required.**

***Index Terms*— Implantable device, neural recording, biomedical integrated circuit, CMOS amplifier, low-offset and low-power, dc offset rejection, velocity selectivity recording (VSR), FPGAs.**

I. INTRODUCTION

The amplitude of the ENG signal is most important for the recording application especially with electrode cuff because the amplitude recorded by this interface technology is very small about 1-5 microvolts, with frequency range from 0.3-5kHz [1-2]. Indeed, this challenge became more difficult with the *multielectrode cuff* (MEC) approach due to the increment in the tripolar amplifiers numbers required in the same area compared with individual tripolar amplifier cuff [3-5]. Furthermore, there are many other challenges facing this approach such as the noise source resistance occurring between the electrodes, the noise generated by the amplifiers itself and dc offset. As a result, a high gain, low noise, minimum dc offset and low power consumption within constricted size limit are the most important boundary conditions[1–5].

Different methods have been used to overcome DC offset challenges such as, auto-zeroing (AZ), correlated double sampling (CDS) and chopper stabilization techniques (CHS) [6-9]. All these approaches are employed in bio-amplifier design to achieve DC offset removal. But, these methods have some weakness points such as they are required a large capacitors in off-chip or on-chip. In addition, these designs increase the CMOS switches number that certainly obtained switching noise and thermal noise, also increase the power consumption. Indeed, these designs were improved the low flicker noise, however they caused higher bandwidth and worse thermal noise performance [10]. Moreover, these approach either on-chip or off-chip application increased the hardware size.

Consequently, we turned to minimize the dc offset in the digital signal processing (DSP) design using online technique for high optimum design and low-hardware cost solution. In this study, a DSP system proposed real time signal processing with low-offset voltage and low-power consumption to meet the essential properties of bio-amplifiers design. The proposed DSP was designed using FPGA board technology, achieved less than 100 µV offset voltage and consumed only 3.5 µW under a 5 V supply. It is a significantly results for ENG signal recording applications.

II. SYSTEM AND CIRCUIT ARCHITECTURE OF VSR METHOD

The method currently in use to estimate the velocity spectrum of ENG data captured by an MEC-based system is based on linear signal processing principles and is referred to as ‘delay and add’ as shown in Fig.1[11-14].

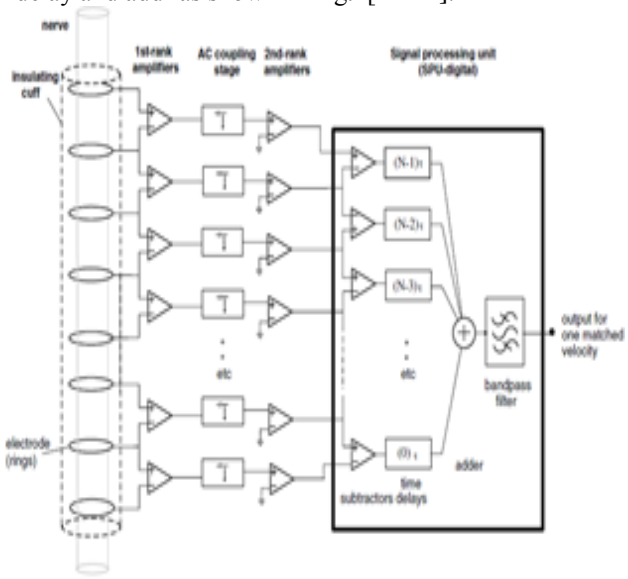

Fig.1. The signal processing unit (SPU) for selecting one velocity (taken from [11]).

The resulting profile of relative signal output as a function of velocity is called the intrinsic velocity spectrum (IVS) [12].

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An Implementation of hardware systems using VSR has been presented in [15], this system implemented in Austria Microsystems 0.8 µm process . Fig.2 shows that the general structure of the system which is consists from two parts, the first part called the electrode unit (EU) which is a mixed analogue/digital signal acquisition system. The second part connected with first part by wires which is called the monitoring unit (MU), both of them are fabricated in 0.8 µm CMOS. Finally, the MU provides the wireless data to external signal processor.

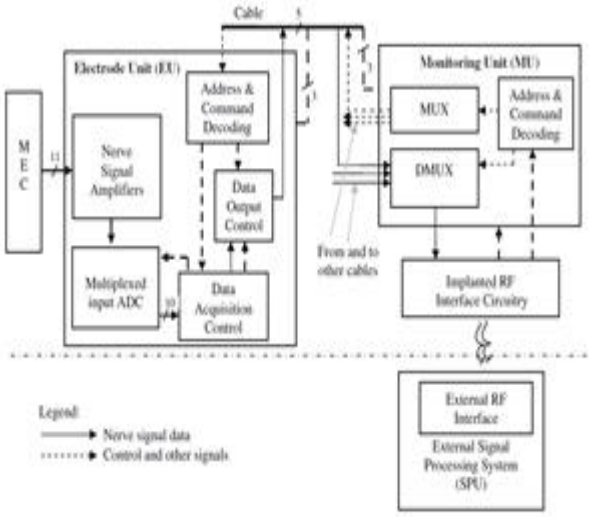

Fig. 2. System construction overview (taken from [15]).

In this research a field Programmable Gate Array (FPGA) have used as a prototype for the design and implementation of signal processing approach for DC offset removal. Since FPGAs offer a flexible and parallel processing supplies and proper for online and high-performance demands. The ability of FPGAs to reconfigure present a significant advantages for online multichannel recording systems, for example dimension and word length of neuronal data, and that make the system changeable and adaptable for various requirements [16].

The FPGAs synthesis and implementation provide high performance, impressive scalability and reconfigurable at the same time compare to other alternative appreoach such as, system-on-chip (SoC) [17]. Consequently, FPGAs have been used for implementation the signal processing system for neural recording application in several studies [18-24].

More attentions have been spent to optimize the circuit design include reduction in the amount of logic gates required and power consumption. Finally, the hardware systems supplying particular circuits for digital signal processing that could considerably replicate the simulation process into real time hardware process. In addition, the hardware solutions are presenting the necessary bio-implantability feature for real-time signal recordings and analysis where these are essential.

III. METHODS

A. Description of General Plan of the System

The block diagram in Fig.3 shows the system which is used to generate an eleven channel simulated AP signal from a multi-electrode cuff with additive noise [21].

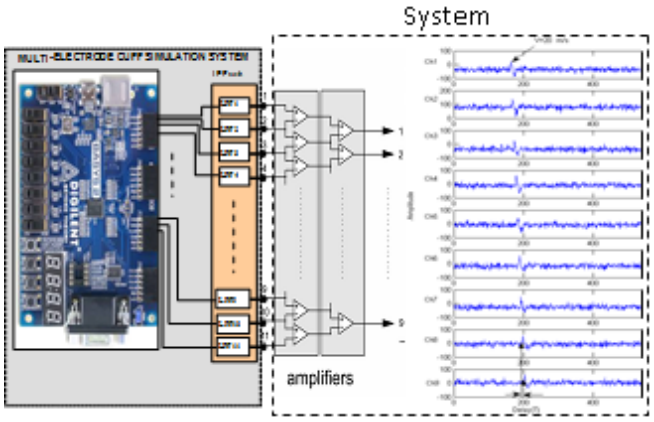

Fig. III: Block diagram of the action potential simulation system with white Gaussian noise[21].

The simulated AP generation system consists of an FPGA based digital controller with a USB interface to a desktop PC. The controller drives a multi-channel low pass filter with a PWM sequence that follows the desired AP waveform. Each channel is skewed in time from the previous channel to simulate the effect of the AP travelling along the nerve bundle as it goes through the multi-electrode cuff. The controller makes use of an off-the-shelf Digilent Basys 2 board which includes a USB interface. Uncommitted digital outputs from the Basys 2 are used as the PWM channel outputs. Each PWM output is connected to an analogue low pass filter that also acts as an attenuator to reduce signal levels and switching noise reaching the system under test on the outputs of the signal simulator [22-24].

The overall plan of the complete system is shown in Fig. 4 and consists of three separate stages. The first stage on the left (block 1) is the programmable AP and noise signal generator (synthesiser) whose output is eleven *unipolar* signals delayed as described in [22-24]. For a typical MEC of length 3 cm the propagation velocity is variable range form 10 – 100 m/s in the A fibre types. To these signals controlled amounts of white Gaussian noise (AWGN) were added in the manner described in chapter three. Blocks 2 and 3 are the two principal sections of a neural recording system intended for ultimate implantation and described in outline in [15]. Block 2 is referred to as the *electrode unit* (EU) and is intended to be mounted on the MEC for optimum performance. It consists of a set of specially designed low noise differential amplifiers whose 10 *bipolar* (or single differential) outputs are digitised (10 bits resolution) and multiplexed into one channel for transmission along an implantable cable [15]. In the architecture described in [15] several EUs are placed at different sites in the peripheral nervous system and connected by implanted cables to a single *monitoring unit* (MU). The MU is a demultiplexer (DMUX) and digital signal processing system that interfaces with an RF telemetry system (not described in this study). In addition to processing and transmitting the recorded data for external logging, the MU processes the system commands and provides power supplies [22-23].

Although a single MU can process the data from and control and power several EUs [15], in the experiments described in this paper only one of each type of unit is used as shown in Fig. 4. In addition, the dc offset removal is a complete prototype is realised in FPGA. Although for ultimate implantation the MU will be a second CMOS ASIC, the comparison of different VSR signal processing strategies

that lies at the heart of this investigation requires easy flexibility of design suggesting the use of FPGA.

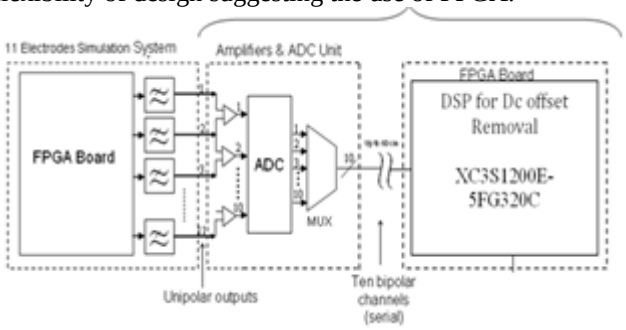

Fig. III. Block diagram of the complete system.

The dc offset removal signal processing circuitry is contained in the unit on the far right of block 3 in Fig. 4 (SPU) and is preceded by stages of de-multiplexing into 10, parallel bipolar channels and conversion into 9 *tripolar* (or double differential) channels (tripolar signals are generally employed in ENG recording applications since they have enhanced immunity to common mode signal contamination (such as *electromyogram*-EMG) compared to monopolar or bipolar ones). Finally the captured and recorded signals are processed for dc removal process. Verilog HDL has been used to syntheses the FPGA board (XC3S1200E-5FG320C) for both approaches under Xilinx –ISE 9.2i platform.

B. The Design and Implementation of DC Offset Removal

In the amplifiers and ADC unit in Fig.4, the DC offset have been measured for ten channels, the all channels have range of DC offset from 0.8-1.1mV. As a result, the delay and add channels have a large amplitude DC offset due to the integration of the DC offset for ten channels, consequently, this increased the hardware size for the digital system implementation, because the signal with high DC Offset will require a large number of bits to represent it. Fig. 5 illustrates the DC offset value for each channel; it is very large compared with the target signal.

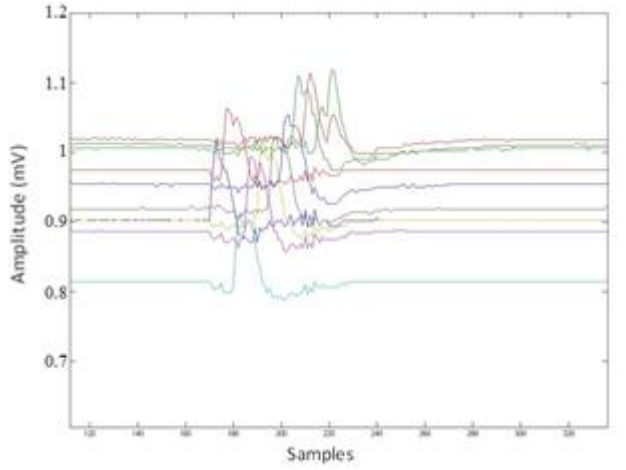

Fig.5. The DC offset value for 9 channels before the DC offset removal.

Each input channel sample from the ADC is 10 bits and the ten channels sample values are combined, so the delay and add output must be 14 bits (see Fig. 6). From fig.6 , we can see clearly the amount of the DC offset value for the delay and add channel (about 1.4mV) compared with peak to peak signal value (about 1.1mV).

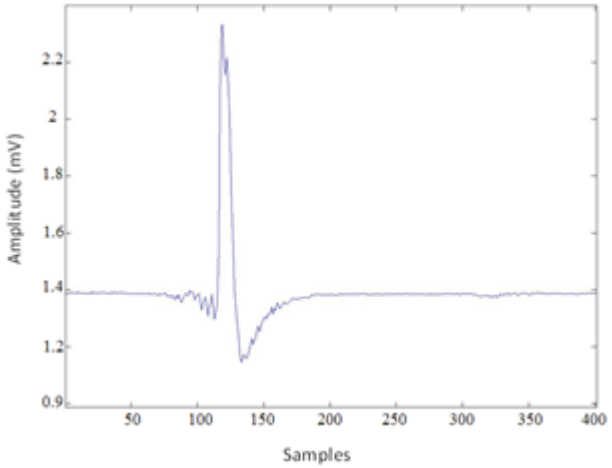

Fig.6. The DC offset value for the delay and add channel before removing the DC offset.

Removal of the DC offset before signal processing results in a significant reduction in the size of memory which is required to save samples from the signal processing data channel.

Table (1) and Fig.6 illustrate the DC offset value for delay and add channel related to temperature and power supply voltage. The result shows a slight variation in the DC offset and this amount of variation cannot be affect on bit number or memory size we have used in digital signal processing system. So if we are supposed the DC offset constant value, the output will has ± very small DC offset depends on variation of temperature and voltage supply. The rest of DC offset can be easily removed with band pass filter in next stage of the system.

Table (1). The DC offset value for delay

Temperature in C°	15 C°	20 C°	25 C°	30 C°	35 C°	40 C°
Supply voltage	0.000298 Dc offset value					
4.5 v	1.35	1.352	1.353	1.361	1.376	1.376
5 v	1.418	1.421	1.4	1.421	1.423	1.418
5.5 v	1.44	1.44	1.433	1.4453	1.437	1.4453

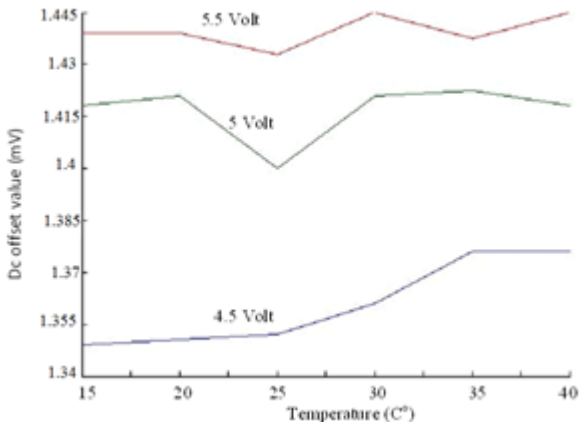

Fig.6.The DC offset variation curve for delay and add channel

Fig.7 shows the procedure which has been followed to reduce number of bit for each sample and for each channel. In the DC offset remover unit the DC offset value is subtracted from the output from each channel which is represented by 9 bit (Fig.7(b)) .This leads to the production an output signal from the signal processing system with very

small (ineffective) value of DC offset within the range of a 10 bit signed number (Fig .7 (c)). The DC offset remover will satisfy our goal of optimizing the memory size for each channel to 6 bits for our application. Clearly, the benefit may be more or less for applications.

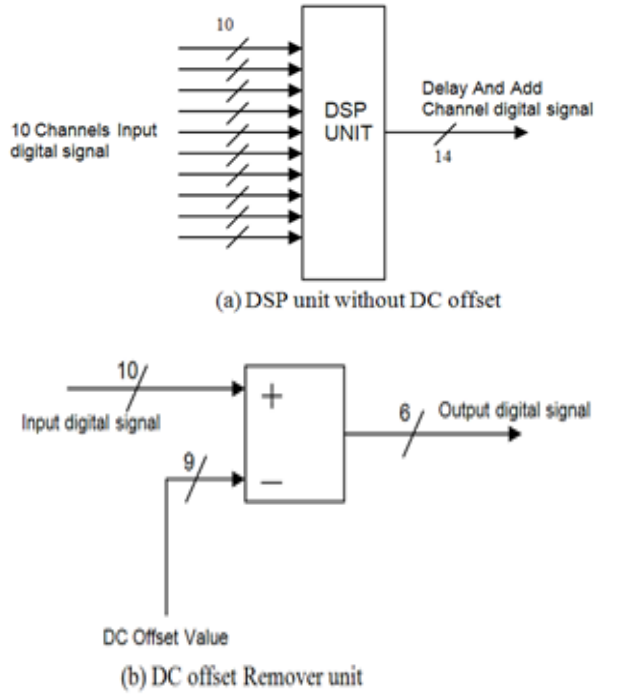

Fig. 7. DSP unit with and without DC offset Remover

A simple circuit can be represented in the digital domain to create a very efficient and practical function of DC remover. The subtraction and multiplexers are all able to operate in 50 MHz which is provided in FPGA board. Therefore, it is also possible to construct a high-performance circuit that is able to capture samples straight from the ADCs.

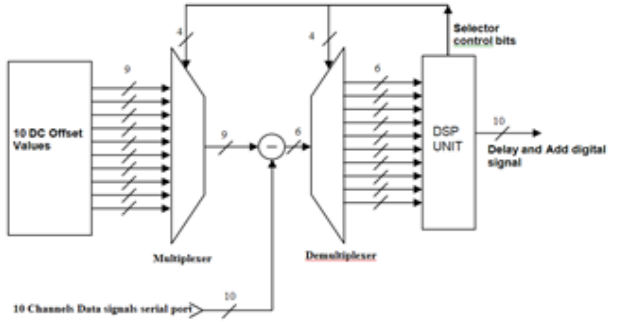

Fig.8 shows how serial processing can assist to remove DC offset thus considerably decreasing the size of hardware. Serial processing can reduce hardware implementation for lower sample-rate applications. In this type of function, the data samples should be supplied in a serial processing; therefore the parallel processing could be transformed to serial processing necessary.

IV. Results and Discussion

Serial processing DC offset remover could be easy implemented with multiplexer and subtraction; the serial implementation needs only one multiplexer and one subtraction to implement 10-bit serial DC offset removal circuit for our application.

This technique demonstrates the strategy of signal processing techniques which could be used effectively in a practical application, it demonstrates possibly to create a high-performance circuit that is able to combine samples directly from ADC using low complexity hardware.

Moreover, the results show how the DC offset value can affected hardware size. The DC offset remover requires a 10 bits subtraction and multiplexer and even the smallest FPGA (Field-programmable gate array) can support more than 10 channels. The size of memories required to store the sample values could easily be supported by block RAMs (Random-Access Memory) on board the FPGA.

In addition, the delay and add channel is considerably reduced by approximate 30% of bits size. Fig.9 shows the delay and add signal after the DC offset removal within the range of a 10 bit signed number.

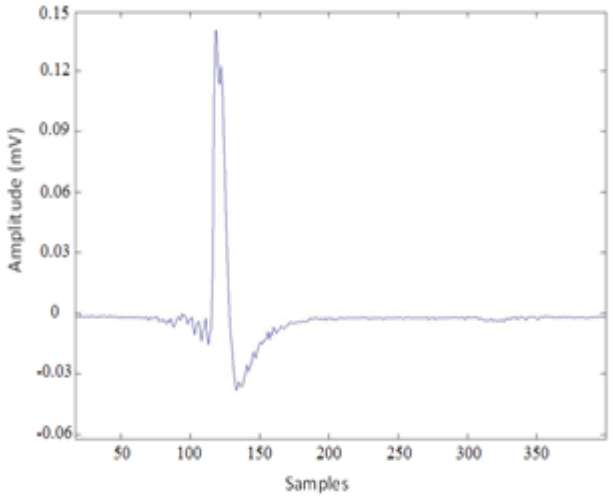

Fig.9. The delay and add channel after removing the DC offset.

In order to test and execute the hardware design, we have employed three methods to implement the system. The first technique has been used in the system which is without DC remover unit and this approach has been employed the BPF filter as DC offset remover as well as its function. Fig.10 shows technique procedure which have been used to implement the system. The second approach it is our method which is describe in detail above (see Fig.11).The third Method have been implement in different structure from previous approaches by setting the DC offset remover between Delay and add channel and BPF (see Fig.12). In this section we evaluate and compare the benefit for our technique against the other techniques. Consequently, we can decide the capability and efficiency of our approach in practical application.

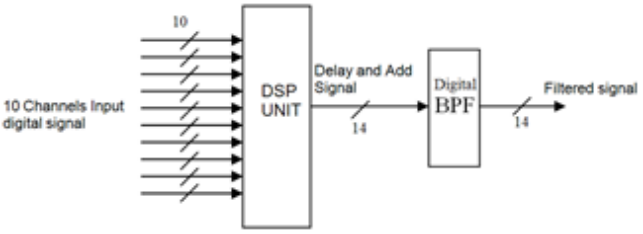

Fig.10. DSP Unit without DC offset removal

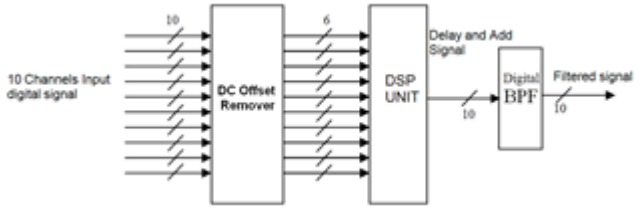

Fig.11. DSP Unit with DC offset remover before channels

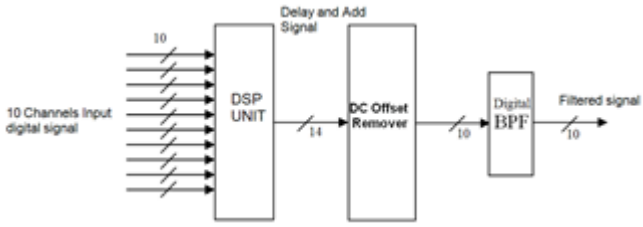

Fig.12. DSP Unit with DC offset remover Delay and add channel.

The all above approaches have been implemented using FPGA board with Xilinx ISE 9.2i software for a 32.5 KHz sample rate and serial process and 50 MHz clock rates. The results show the amount of interest design that have been obtained after the implementation of the two methods, it is clear in Table(2) the amount of gates and slices that are save in our technique of comparison with conventional method where the provision of 35819 gates and 113 slices, in addition we save 1 MB from internal FPGA memory. This is significant indicator of the effectiveness and efficiency of our approach, including qualifies it to be a practical and applicable method.

Table (2) Device utilization summary for three methods

Method Name	Without DC offset	With DC offset removal
Number of Slices	608 out of 8672 7%	495 out of 8672 5%
Number of Slice Flip Flops	520 out of 17344 3%	419 out of 17344 2%
Number of 4 input LUTs	1040 out of 17344 6%	819 out of 17344 4%
Number of bonded IOBs	30 out of 250 12%	25 out of 250 10%
Number of BRAMs	11 out of 28 40%	10 out of 28 35%
Number of MULT18X18SIOs	27 out of 28 95%	26 out of 28 92%
Number of GCLKs	1 out of 24 4%	1 out of 24 4%
Total equivalent gate count for design	701,683	665,864
Peak Memory Usage	166 MB	165 MB

The ADC and preamplifier unit which has been used in our design has operating DC power supply range from 4.5V to 5.5V DC. In order to determine the temperature effect on the DC offset value we are set some of experiments to calculate the DC offset value at different temperature value.

The full hardware system after implementation and verification is shown in Fig. 13 which includes electrode simulation unit, amplifiers and ADC unit and the DSP unit. The DSP unit is used for processing the dc offset removal for the data in both conventional and TDNN approach which have been synthesised and implemented on the same FPGA board. Indeed, the flexibility of the FPGA allowed reconfiguring and generating multi- prototype implementations designs using only one FPGA board. This advantage of choosing FPGA for implementation target is saving the efforts, time and cost during prototype design. Also, generation multi- prototypes for both approaches provide a wide selection options to have fair comparison among these implementation methods without needing to redesign the system each time because it is easy to upload them and running at any time. In fact, this FPGA future cannot be easy offer with alternative technologies. Moreover, the cost itself is very reasonable and efficient for producing a prototype task.

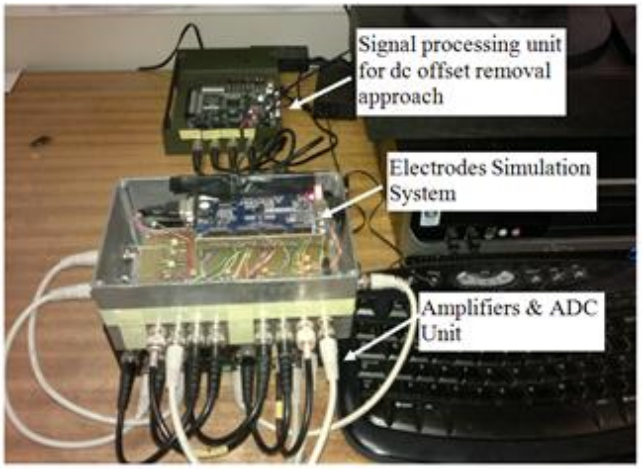

Fig. 13: The hardware system constructions for the complete design

V. Conclusion

This study proposed an analysis circuit configuration demonstrate that this approach could achieve a small DC offset error (less than 100µV), with small size required. A low-offset low-power and low hardware cost with online DC offset removal design technique for VSR method in nerve activities recording applications is presented in this paper, without hardware cost to enhance the circuitry ability over power supply and temperature. The system process obtained using this approach having a 10-bit signal processing for DAC resolution, with 1.4 mA rms output current, with minimum size around 0.02 mm^2 of chip area. The FPGA board has been used as a prototype for the design and implementation the dc offset signal processing approach. The whole circuit configured in FPGA board and consumed only 495 Slices from the FPGA board hardware area and the completed system consumed 665,864 gate while the system without dc offset removal consumed 701,683 gate. In addition, the dc offset removal reduces the dc offset value to be less than 100µV, which was 1.4mV in conventional method.

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