Efficient reduction of leakage power in low power VLSI circuits using Sleepy Keeper Approach

Monisha.S, Priya.M, A. Upendra Raju, Uma.V

***Abstract*— Voltage Scaling in CMOS circuits will reduce the threshold voltage, however there is an increase in the sub threshold leakage current and hence static power dissipation. This increase in leakage power dissipation is a concern in VLSI design even for the most recent CMOS feature sizes. To reduce this power dissipation an approach called sleepy keeper is used for CMOS circuits. This approach uses two additional transistors along with the traditional sleep transistors. These additional transistors help to save a logic state during the sleep mode.**

***Index Terms*— Subthreshold leakage power, Static power, Dynamic Power, Propagation delay, Sleep transistors.**

I. Introduction

A major concern in CMOS circuit design is the power consumption. Power consumed by a CMOS circuit consists of dynamic and static components. Dynamic power is the power consumed by the circuit when transistors are switching, whereas static power is the power consumed by the circuit irrespective of transistor switching.

Earlier dynamic power consumption was a single major concern for low power VLSI circuit designers as it accounted for 90% or more of the total circuit power. Hence scaling techniques such as voltage and frequency scaling focused only on dynamic power reduction.

However, as the feature size reduces to 65nm, 45 nm and less, static power has become a major challenge for current and future technologies. According to the International Technology Roadmap for Semiconductors (ITRS), the subthreshold leakage power dissipation of a chip may exceed dynamic power dissipation at the 65nm feature size. To address this static power dissipation problem, many researchers in the past and present have proposed different ideas from the device level to the architectural level and above [1,2]. These techniques include sleep, zigzag, stack and sleepy stack for leakage power reduction. Each approach has its own advantage and disadvantage in reducing leakage power.

In this paper, an approach called sleepy keeper is used for reducing leakage power. In this approach, static power, dynamic power and leakage power is reduced when compared to other approaches. Power delay product is also less when compared with all the other approaches [3]. Tanner EDA tool has been used for designing the circuits and for calculating the static power, dynamic power, and delay for all the approaches.

Monisha.S, Department of Electronics, Mount Carmel College, Bangalore
Priya. M, Department of Electronics, Mount Carmel College, Bangalore
A.Upendra Raju, Department of Electronics, Mount Carmel College, Bangalore
Uma.V, Department of Electronics, Mount Carmel College, Bangalore

II. Leakage Power Reduction Approaches

A. Sleep Approach

In the sleep approach, transistors gating V_{DD} and V_{SS} are added to the base case. The power supply will be cut-off for these added transistors when in sleep mode. Each added transistor is called as a sleep transistor and takes the width of the largest transistor in the base case. As shown in Fig. 1 a PMOS sleep transistor is placed between V_{DD} and the pull-up network, and an NMOS sleep transistor is placed between V_{SS} and the pull-down network. The sleep transistors are driven by Sleep (S) and Sleep'(S') signals.

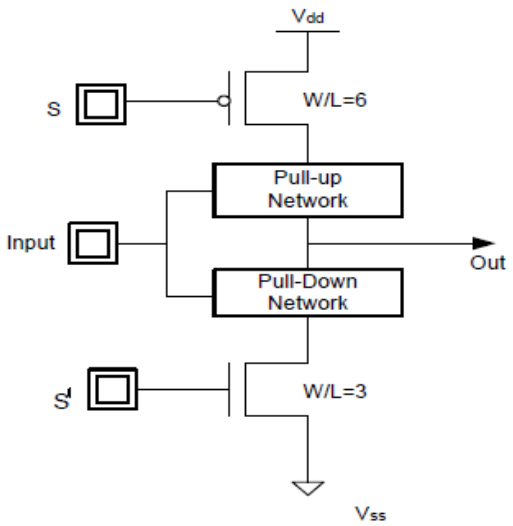

Fig. 1. Sleep Approach

The two sleep transistors will disconnect the circuit from V_{DD} and V_{SS} when the logic circuit is in sleep mode. This technique can reduce the leakage power effectively, by removing power to the circuit during sleep mode. However, after sleep mode the output of the circuit will be floating and there is destruction in the output state because of the wake-up delay of sleep transistors [4].

B. Zig-Zag Approach

To remove the floating state of the circuit by reducing the wake-up delay of sleep transistors, the zigzag technique has been introduced as shown in Fig.2. This technique reduces the wake-up delay by choosing a particular output state for the circuit and then turning off the pull-down circuit for each gate whose output is high and turning off the pull-up circuit for each gate whose output is low. If the chosen output is '1', then a pull-down sleep transistor is added and if the chosen output is '0', then a pull-up sleep transistor is added. Prior going to

chip fabrication, by choosing a particular input pattern the zigzag technique can prevent floating of the output.

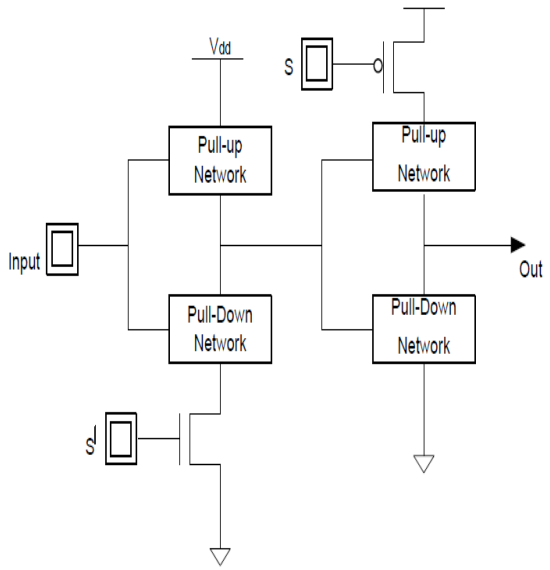

Fig. 2. Zig-Zag Approach

Zigzag technique retains the prior chosen state but any other arbitrary state appears during regular operation will be lost during power down mode of the circuit. Also this approach needs an extra circuitry for generating a specific input pattern [4].

C. Stack Approach

In stack approach, every transistor is duplicated with two transistors of original type bearing half the width of original transistor as shown in Fig.3. These duplicated transistors cause a reverse bias between the gate and the source when both of them are in cut-off. Due to this, a substantial reduction in sub-threshold current, as it depends exponentially on the gate bias.

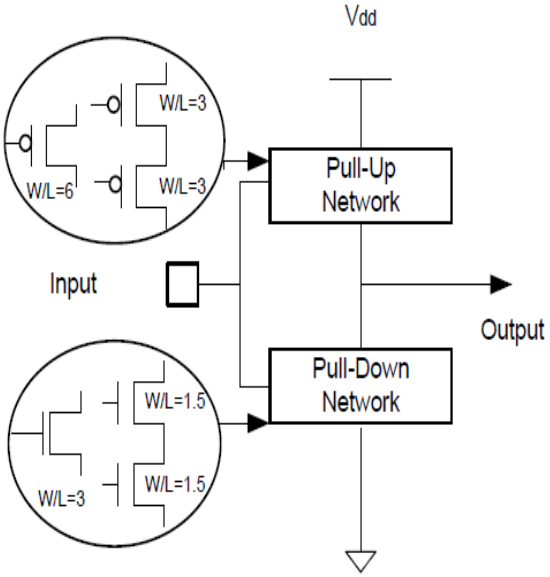

Fig. 3. Stack Approach

In this approach, all transistors are placed in-between two parallel rows of V_{DD} and V_{SS}, hence increase in number of transistors and decrease in transistor width which will in turn increases the delay significantly and could limit the usefulness of the approach [4].

D. Sleepy Stack Approach

This approach is a combination of the stack and sleep approaches by dividing every transistor into two transistors of half width and placing a sleep transistor in parallel with one of the divided transistor, as shown in Fig.4

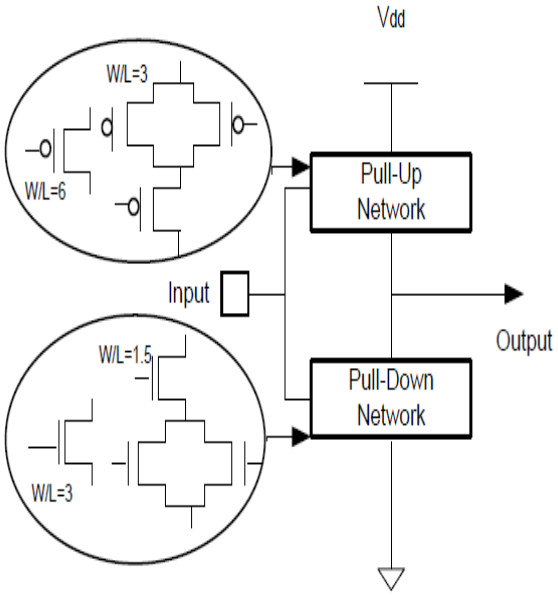

Fig. 4. Sleepy Stack Approach

The stacked transistors will suppress the leakage current while saving a state. Each sleep transistor placed in parallel to the stacked transistors, reduces resistance of the path, so that delay is reduced during the active state. However, area occupied by this approach is more because every transistor is replaced by three similar transistors.

To summarize, sleep approach is capable of reducing leakage power but suffers from destruction of state and floating output voltage. The destruction of state is eliminated in the zigzag approach but still floating output voltage problem exists. The stack approach suffers from increased delay and the sleepy stack approach consumes more area. Hence an approach called sleepy keeper approach is used to overcome some of these disadvantages.

III. SLEEPY KEEPER APPROACH

The structure of the sleepy keeper approach is as shown in Fig.5. This approach has the advantage of ultra-low leakage power, capability of state-saving, occupies less area and faster than the sleepy stack approach. The design of NAND gate using sleepy keeper approach is shown in Fig.5. For the sleep, zigzag and sleepy, dual threshold voltage (V_{th}) technology can be applied to obtain greater leakage power reduction. Since high-V_{th} results in less leakage but lowers the performance, high- V_{th} is applied only to leakage reduction transistors, which are sleep transistors, and any transistors in parallel to the sleep transistors; on the other hand, low-V_{th} is applied to the remaining transistors to maintain logic performance [4].

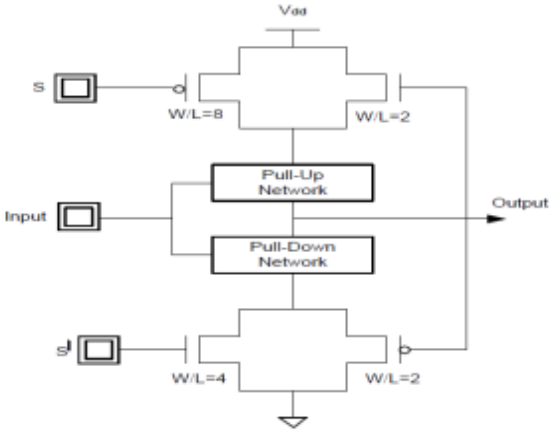

Fig. 5. Sleepy Keeper Approach

IV. RESULTS AND DISCUSSIONS

A. Results

In order to compare the results of the sleepy keeper approach with other leakage power reduction approaches like, stack, sleep, zigzag, and sleepy stack approaches simulations are carried out considering NAND gate as a base case.

Table 1: Results for NAND gate (1.25 µm)

Approaches	Area (m²)	Delay (sec)	Static power (Watts)	Dynamic power (Watts)	Total power (Watts)	Power delay product
Sleep approach	1.17E-06	2.39E-09	1.95E-12	1.27E-03	1.27E-03	3.02E-12
Stack approach	7.76E-07	2.81E-09	5.15E-12	9.20E-04	9.20E-04	2.59E-12
Zigzag approach	9.72E-07	2.28E-09	1.55E-12	1.04E-03	1.04E-03	2.37E-12
Sleepy stack approach	1.17E-06	2.73E-09	6.25E-12	9.75E-04	9.75E-04	2.66E-12
Sleepy keeper approach	6.80E-07	2.65E-09	3.75E-13	7.30E-04	7.30E-04	1.93E-12

Table 2. Results for NAND gate (65nm)

Approaches	Area (m²)	Delay (sec)	Static power (Watts)	Dynamic power (Watts)	Total power (Watts)	Power delay product
Sleep approach	114.075E-15	2.23E-09	2.957E-09	147.33E-09	150.287E-09	0.33512E-15
Stack approach	101.4E-15	2.925E-09	12.090E-09	121.33E-09	133.42E-09	0.39025E-15
Zigzag approach	76.05 E-15	2.52E-09	9.287E-09	146.33E-09	155.617E-09	0.39215E-15
Sleepy stack approach	114.075 E-15	3.385E-09	16.062E-09	129.33E-09	145.392E-09	0.492151E-15
Sleepy keeper approach	66.54 E-15	2.375E-09	3.855E-09	79.33E-09	83.185E-09	0.1975E-15

Table 3. Results for NAND gate (45nm)

Approaches	Area (m²)	Delay (sec)	Static power (Watts)	Dynamic power (Watts)	Total power (Watts)	Power delay product
Sleep approach	67.5E-15	3.655E-09	2.202E-09	80.153E-09	82.355E-09	0.301E-15
Stack approach	45E-15	6.815E-09	2.531E-09	62.7E-09	64.731E-09	0.441E-15
Zigzag approach	60E-15	4.42E-09	5.06E-09	80.7E-09	85.76E-09	0.379E-15
Sleepy stack approach	67.5E-15	4.85E-09	5.833E-09	67.7E-09	73.553E-09	0.356E-15
Sleepy keeper approach	39.375E-15	3.315E-09	2.5E-09	59E-09	61.5E-09	0.203E-15

B. Discussions

Data in Tables 1 to 3 are represented graphically in the following. The sleepy keeper approach consumes less area when compared to other approaches. As the feature size of the transistor scales down the area consumed reduces as shown in Fig.6 & Fig.7, which increases the component density in VLSI circuits.

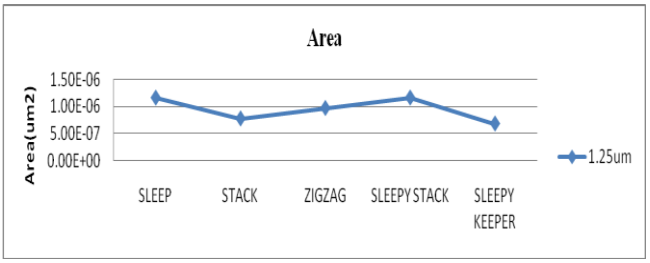

Fig. 6. Area of NAND gate (1.25µm)

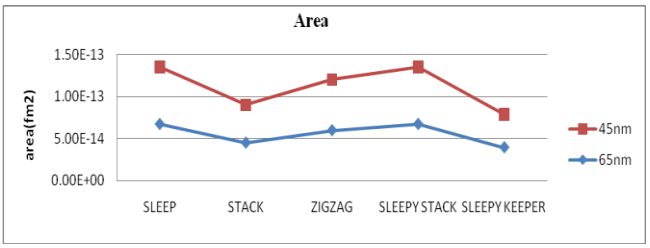

Fig. 7. Area of NAND gate (65nm & 45nm)

As the feature size of transistor scales down, the static power consumption increases as shown in Fig.8 & Fig.9. If this increase in power consumption proceeds there is a possibility that it may exceed dynamic power consumption. As a solution to the above problem sleepy keeper approach is used which results in low static power consumption.

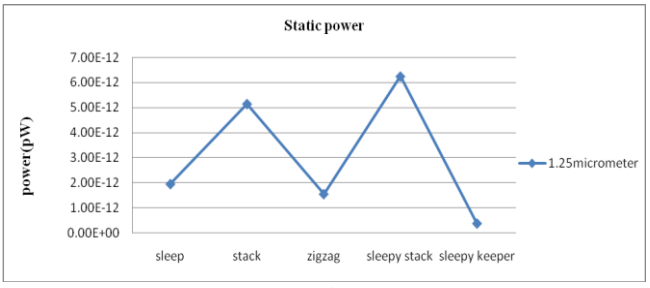

Fig.8. Static Power of NAND gate (1.25µm)

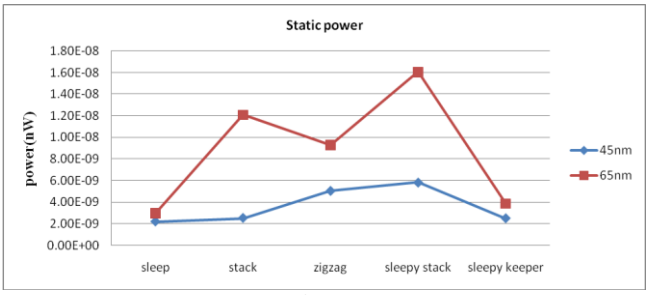

Fig. 9. Static Power of NAND gate (65nm & 45nm)

There is less dynamic power dissipation in sleepy keeper approach when compared with other approaches as shown in Fig.10 & Fig.11. It is also seen from these figures that as the feature size of transistor scales down, the dynamic power dissipation also decreases.

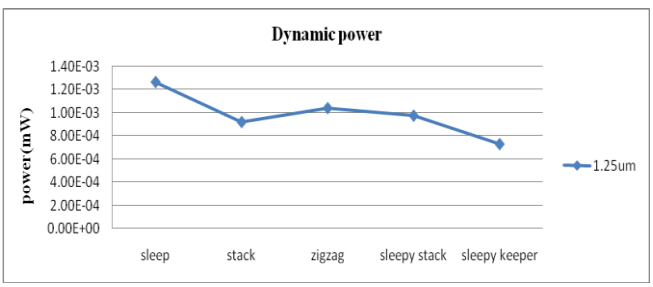

Fig. 10. Dynamic Power of NAND gate (1.25µm)

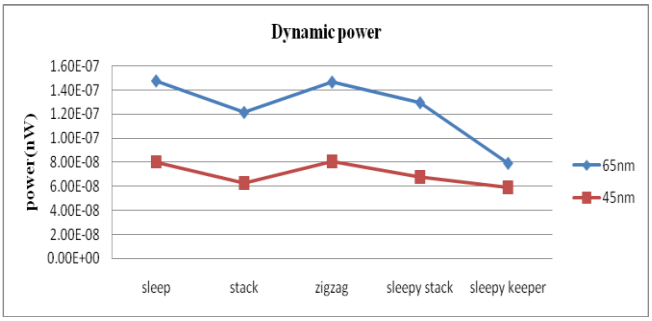

Fig.11. Dynamic Power of NAND gate (65nm & 45nm)

As the technology scales down, the supply voltage given to the circuit reduces. Hence the propagation delay increases with this reduction in the power supply voltage as shown in Fig.12.

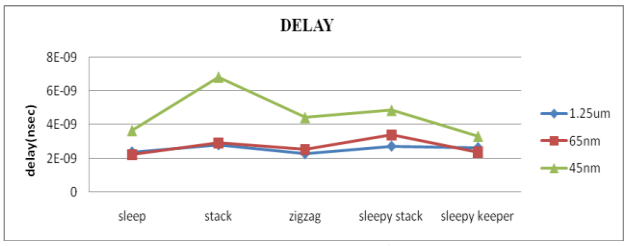

Fig.12. Propagation Delay of NAND gate

V. CONCLUSIONS

Scaling down of the CMOS technology feature size and threshold voltage for achieving high performance has resulted in increase of leakage power dissipation.

This paper emphasis on reducing leakage power in VLSI design using an efficient methodology “Sleepy Keeper Approach”. In case of sleepy keeper approach, static power, dynamic power dissipation and power delay product is less when compared with all the other approaches.

It is seen that the delay and the static power is found to increase as the technology scales down. Hence, as a solution sleepy keeper approach is used and this approach reduces delay and static power considerably.

REFERENCES

[1] Hina malviya, Sudha Nayar, C.M Roy, “A NEW APPROACH FOR Leakage Power Reduction Techniques in Deep Submicron Technologies in CMOS CIRCUIT for VLSI Applications” International Journal of Advanced Research in Computer Science and Software Engineering Volume 3, Issue 5, May 2013.

[2] Jun Cheol Park, “Sleepy Stack: a New Approach to Low Power VLSI Logic and Memory” School of Electrical and Computer Engineering Georgia Institute of Technology August 2005.

[3] K. Gnana Deepika, K. Mariya Priyadarshini, K. David Solomon Raj, “Sleepy Keeper Approach for Power PerformanceTuning in VLSI Design” International Journal of Electronics and Communication Engineering Volume 6, Number 1 (2013), pp. 17-28.

[4] P.Srikanth, Prof.R.Ramana Reddy, “Design of Ultra-low Leakage Power Sequential Circuits” Int.J.Computer Technology & Applications,Vol 3 (3), pp.1254-1259.